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MS-7756

m-ATX H/W:JaysonChen
Ver: 1.0(243.84 * 243.84) PM:BobbyYuan

Intel -MahoBay plamform H77

CPU: *IVY bridge LGA1155*

System Chipset: *Panther Point H77*

Onboard Chip:

HD Audio Codec:ALC892 colay 887
LAN-RTL8111E colay8105E
SIO:Fintek F71868AD
Flash ROM: SPI 64 MB

Main Memory:

*DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)*

ACPI: *UPI*

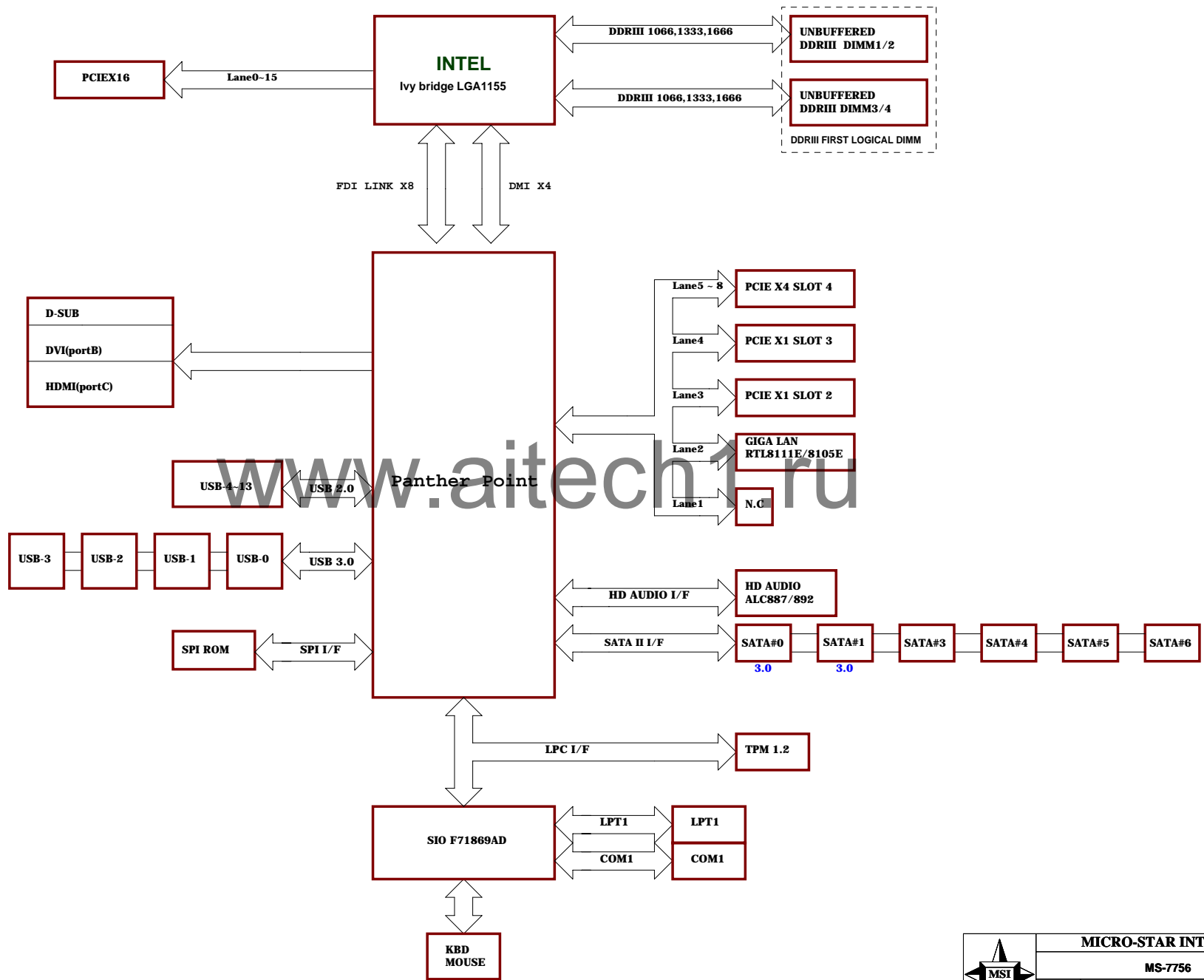
PWM: *VRD12 -UT501 3+1 Phase*

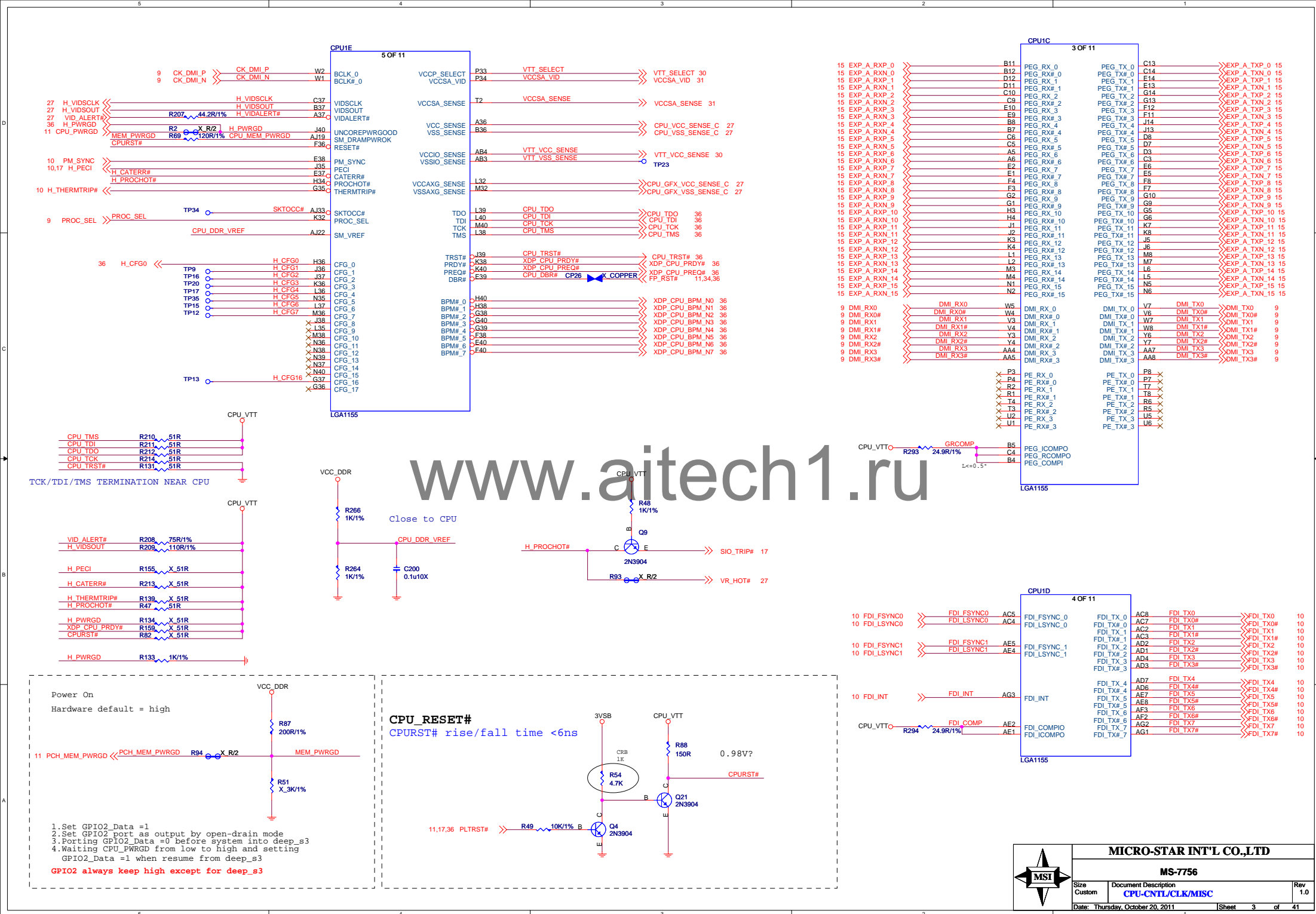
Expansion Slots:

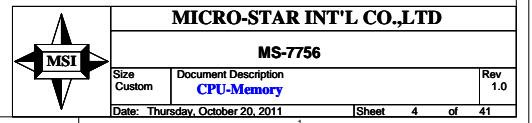
*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2*
*PCI Express (X4) Slot * 1*

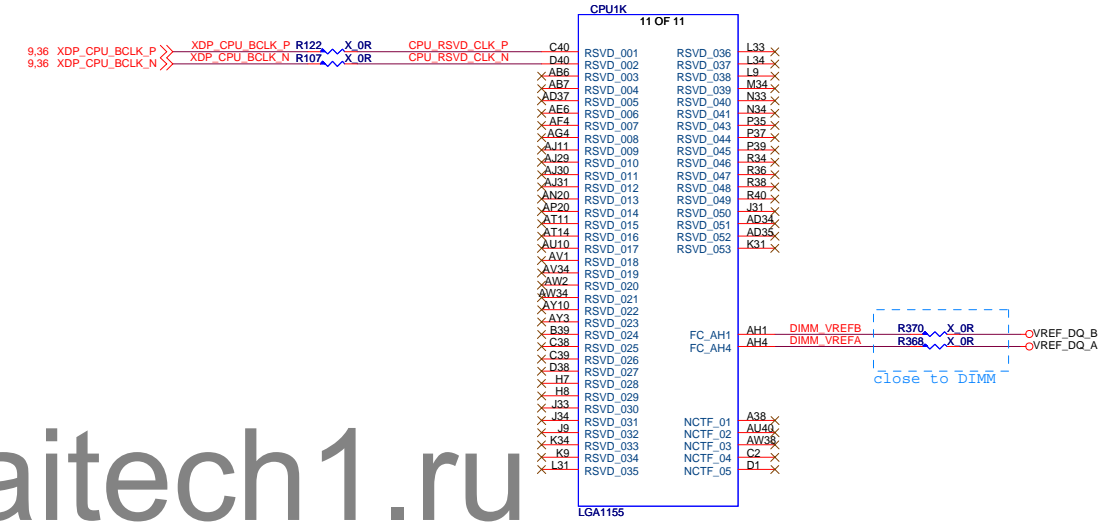
Other: *SATA3.0 x2+SATA2.0 x4 (PCH)*
*USB2.0 *10*
*REAL USB3.0 *2*
*FRONT USB3.0 *2*

MS-7756 Block Diagram





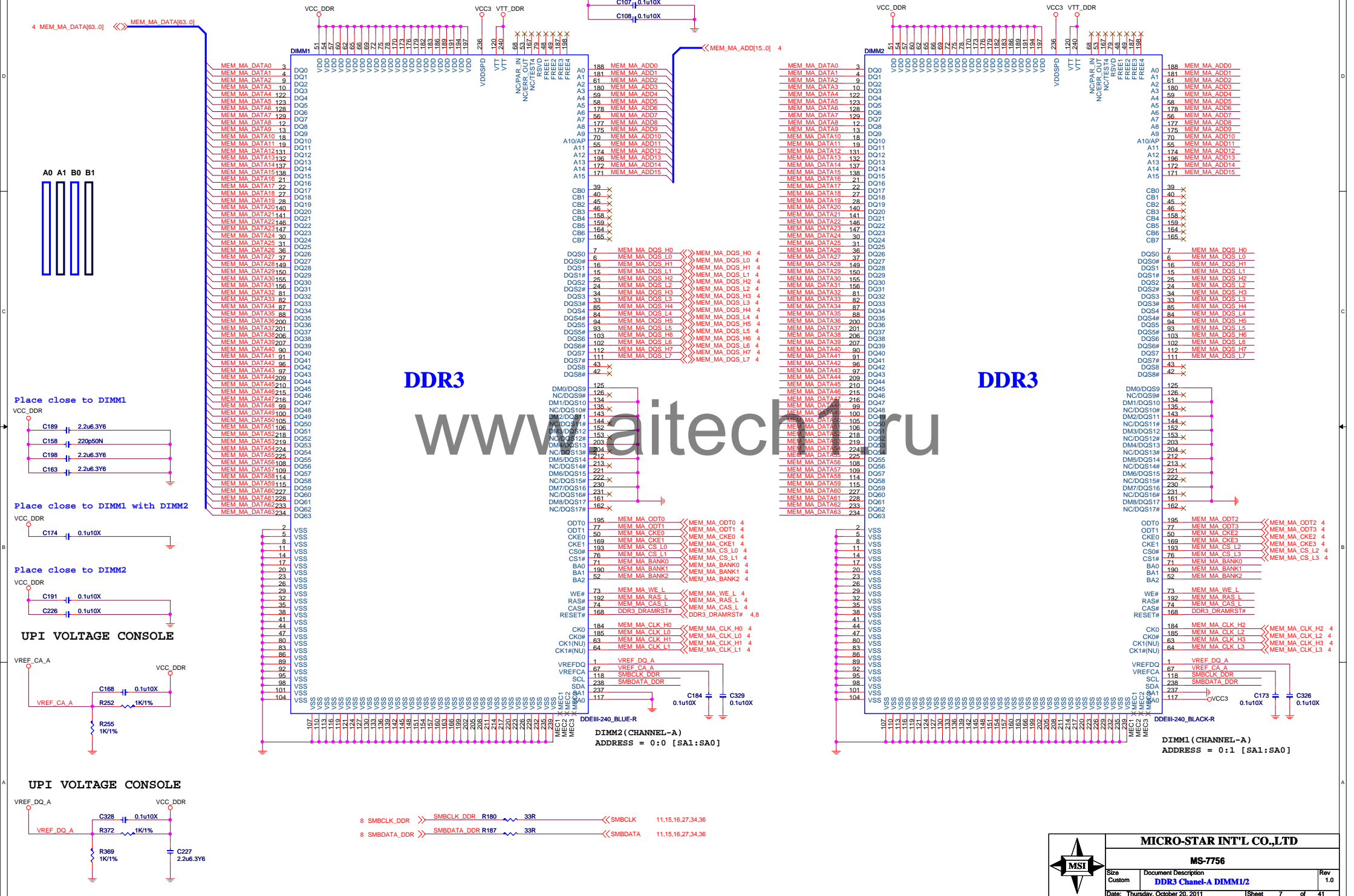




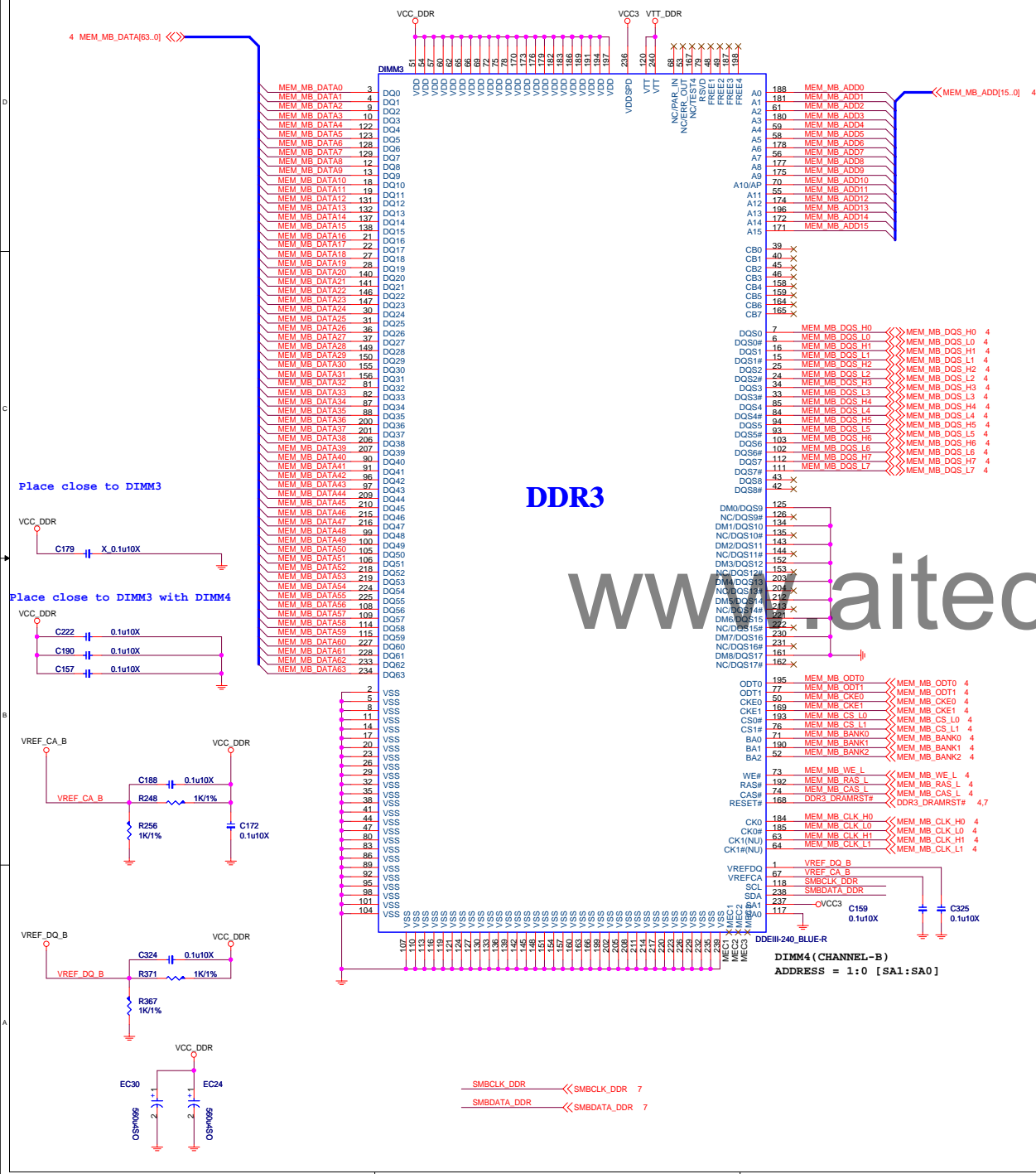
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DDRIII DIMM_A0

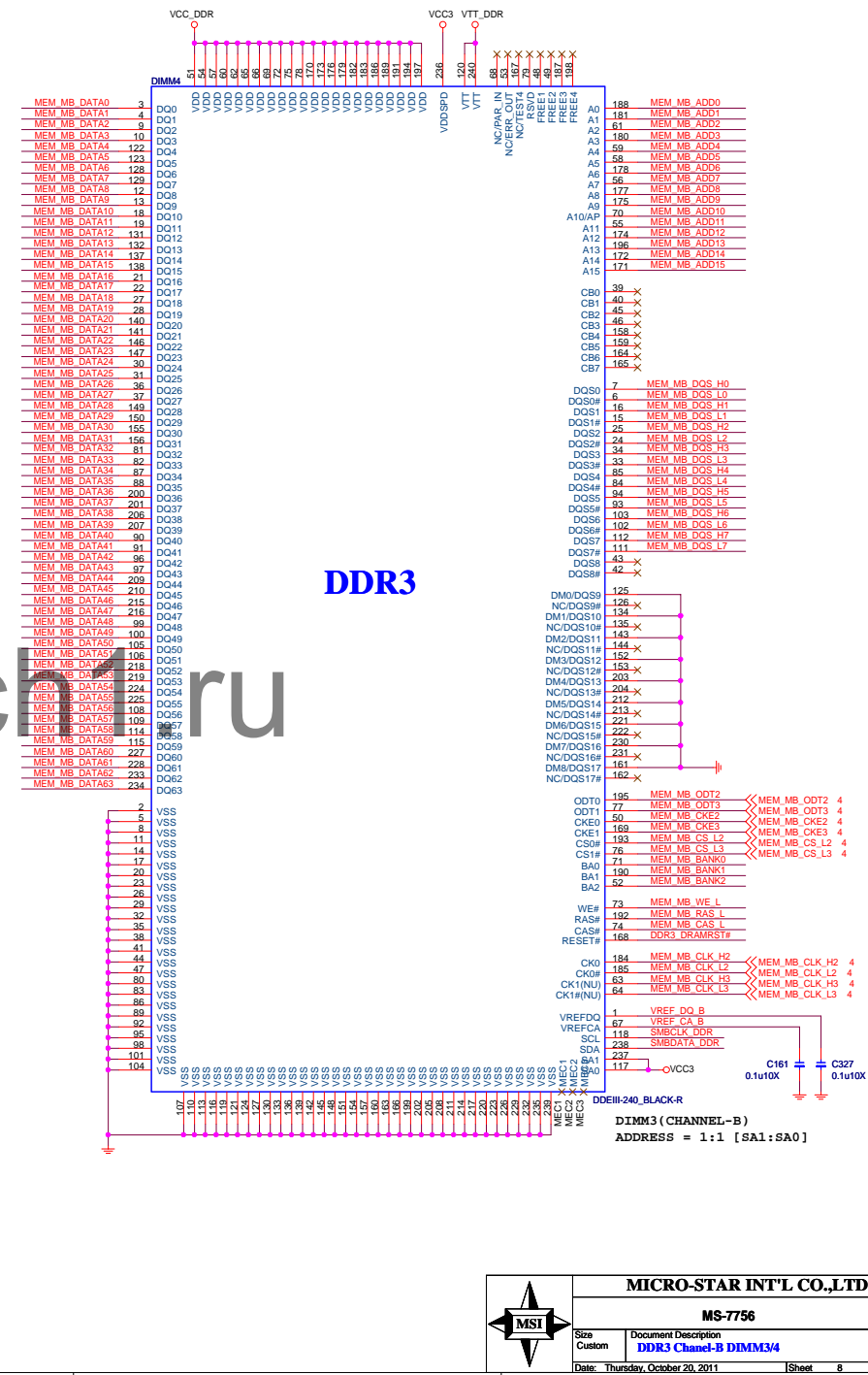
DDRIII DIMM_A1



DDRIII DIMM_B0



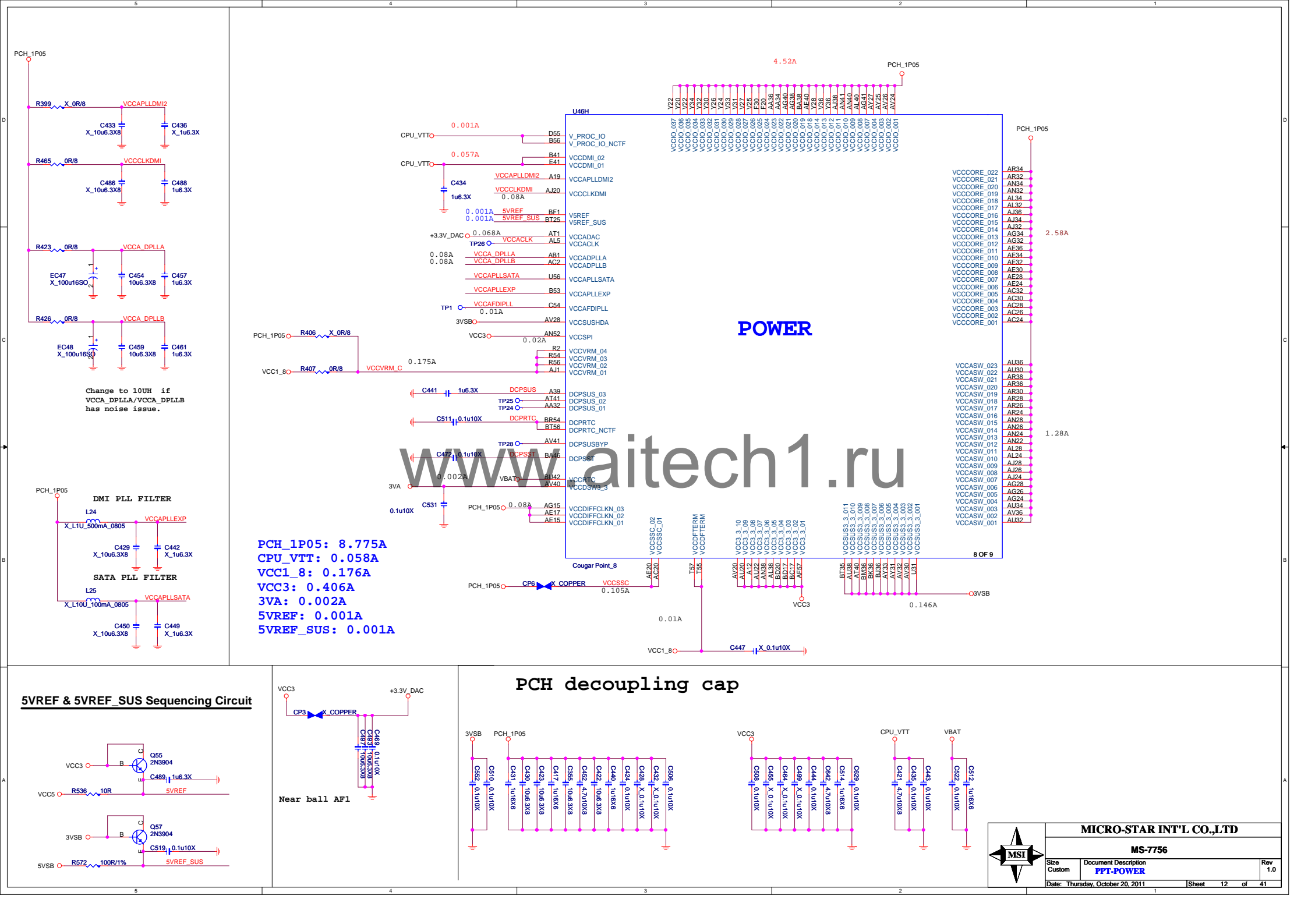
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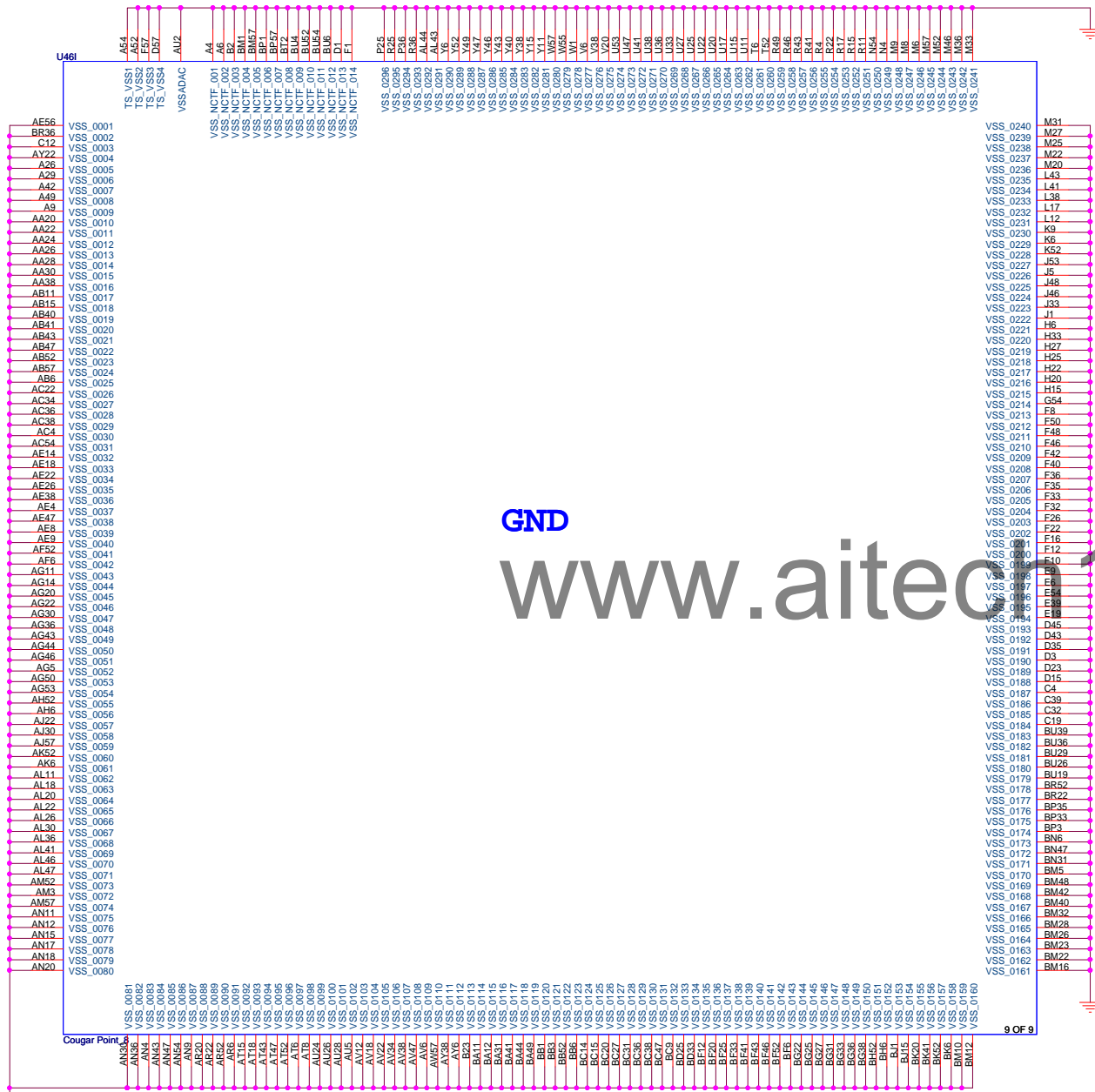


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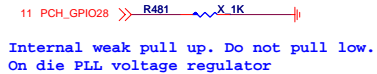
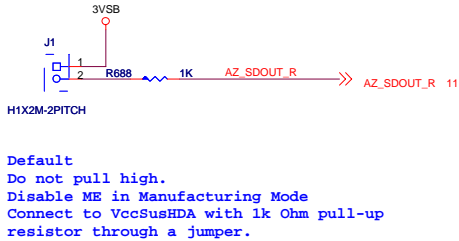
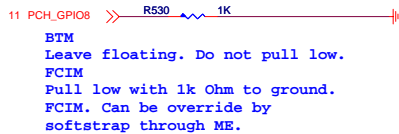
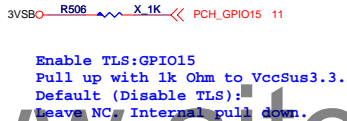
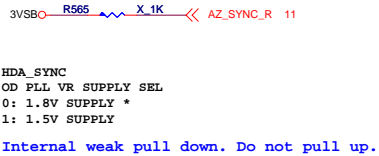
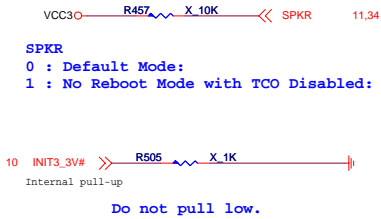
MS-7756

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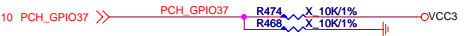




PCH Straps



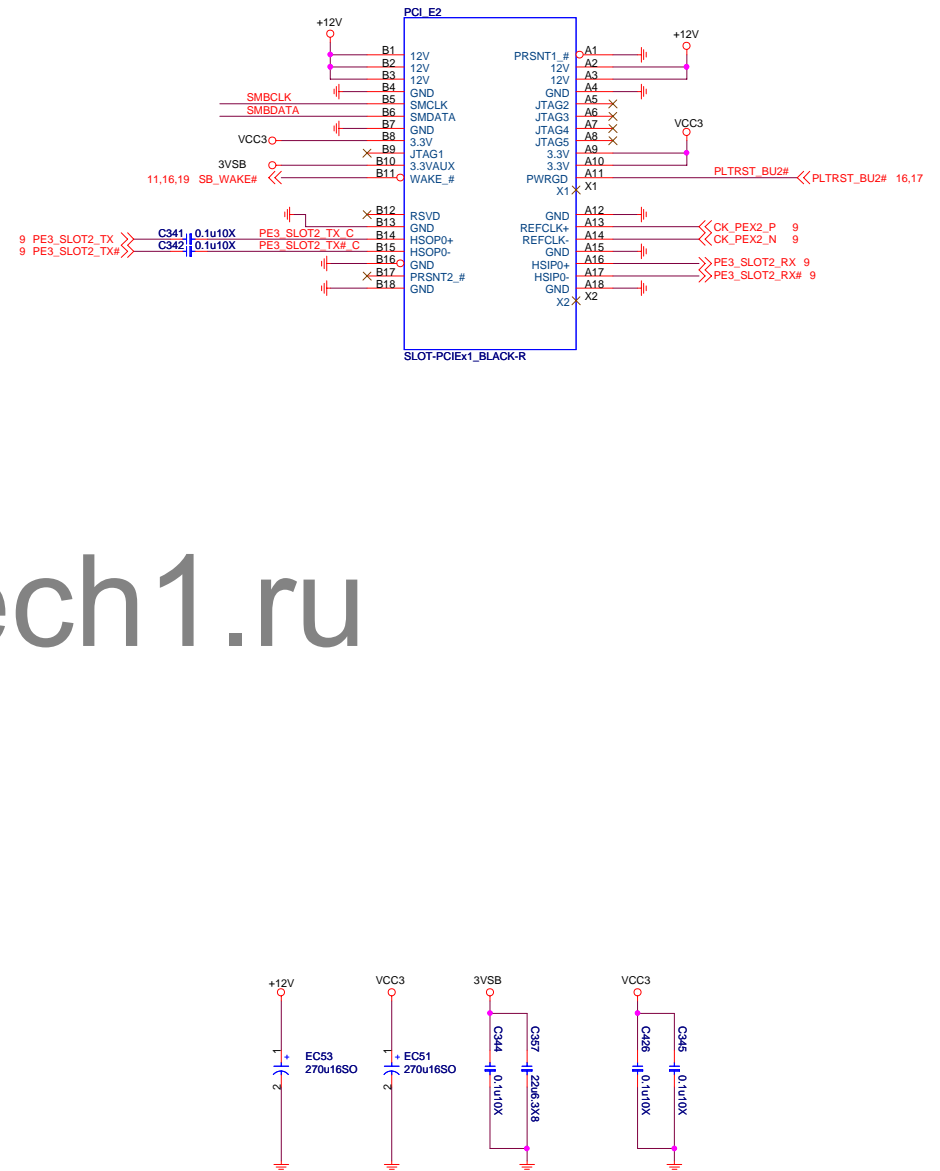
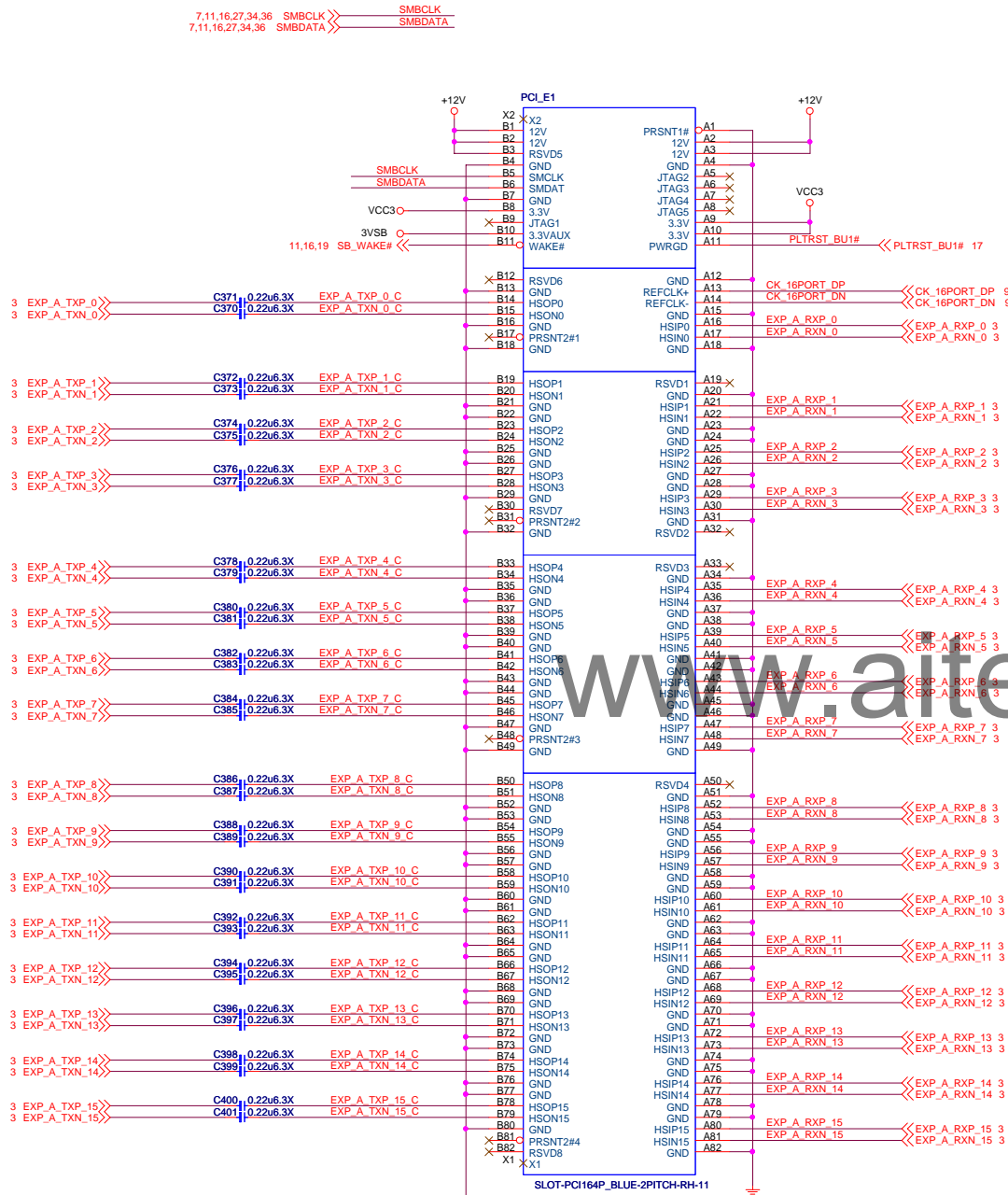
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.



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When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.



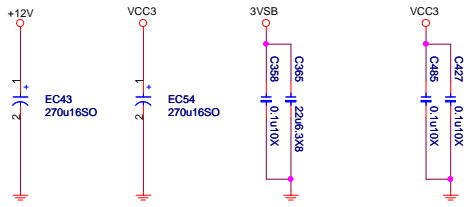
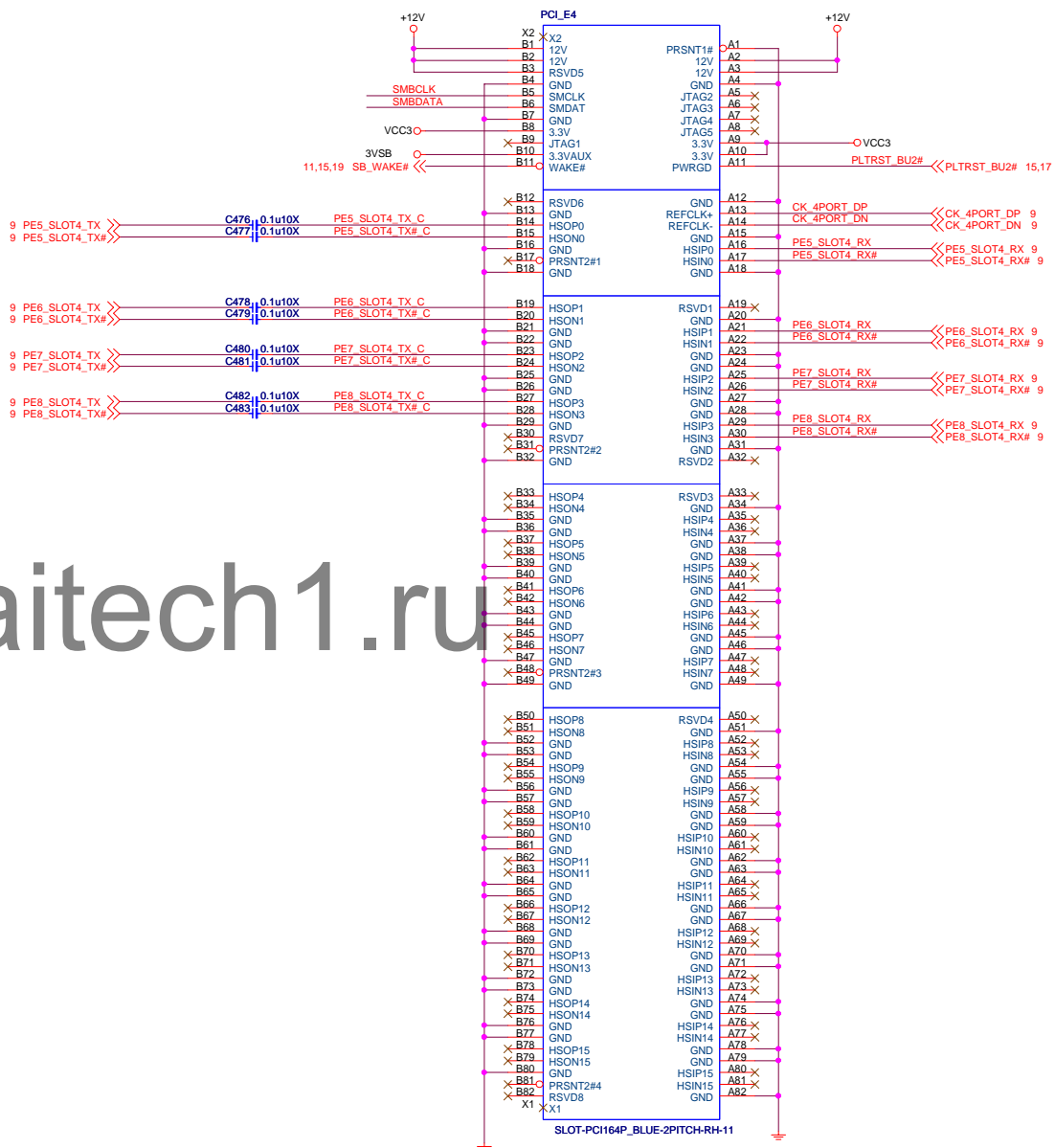
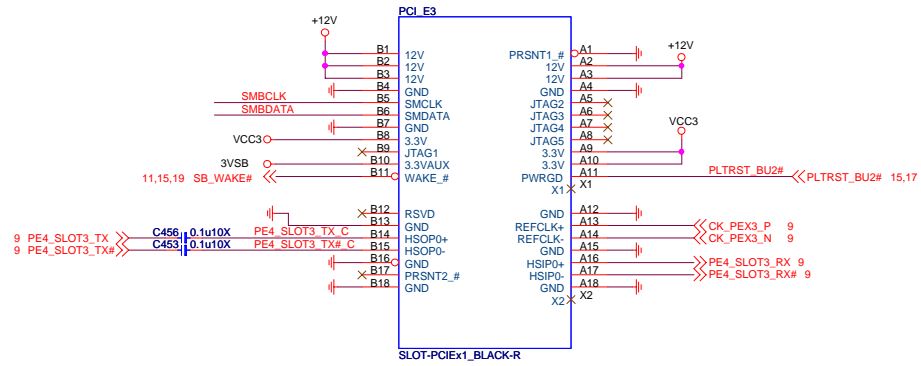
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MS-7756		
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7,11,15,27,34,36 SMBCLK
7,11,15,27,34,36 SMBDATA

SMBCLK
SMBDATA

PCI Express X4 Slot



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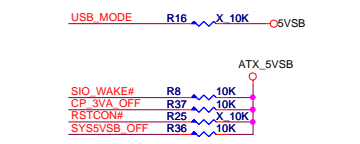
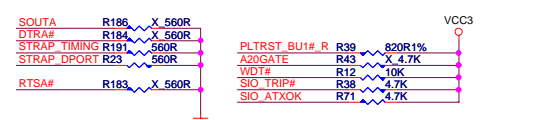
MICRO-STAR INT'L CO.,LTD		
MS-7756		
Size	Document Description	Rev
Custom	PCIE3(X1) & PCIE4(X4) Slots	1.0
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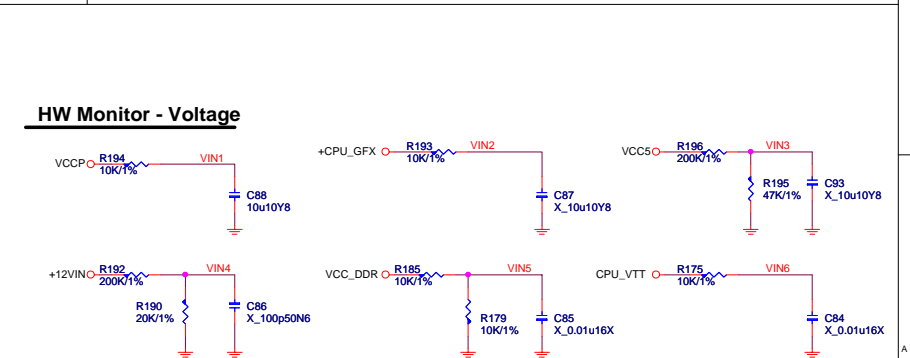
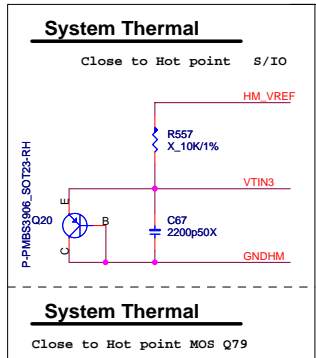
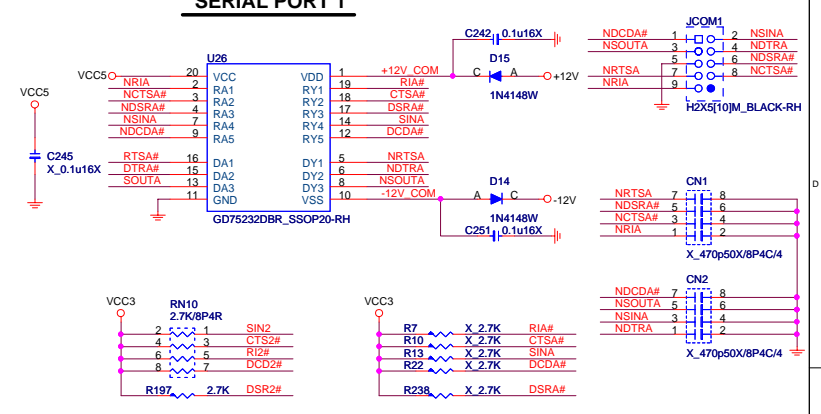
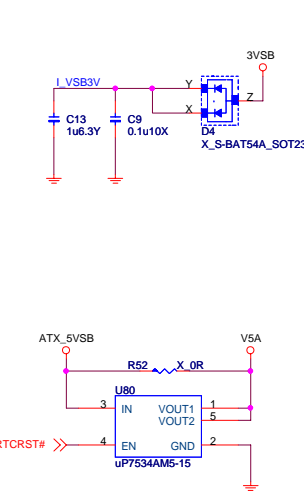
LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

USB_MODE
Hi by BIOS programming,
default h/w PD for avoid UP7536 Enable pin floating

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Couragar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		

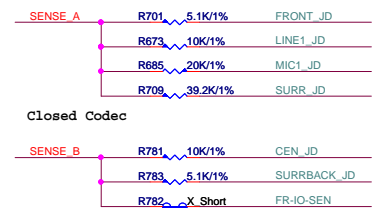
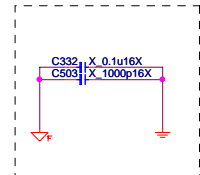


GPIO34 / GPIO33 / GPIO32	0	1	0
	0	0	1
	0	1	0

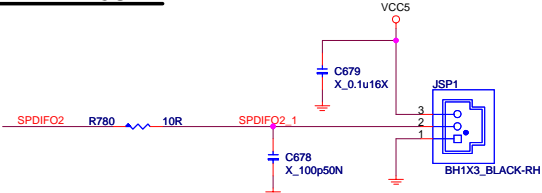


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SIO-Fintek F71869AD
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ALC892



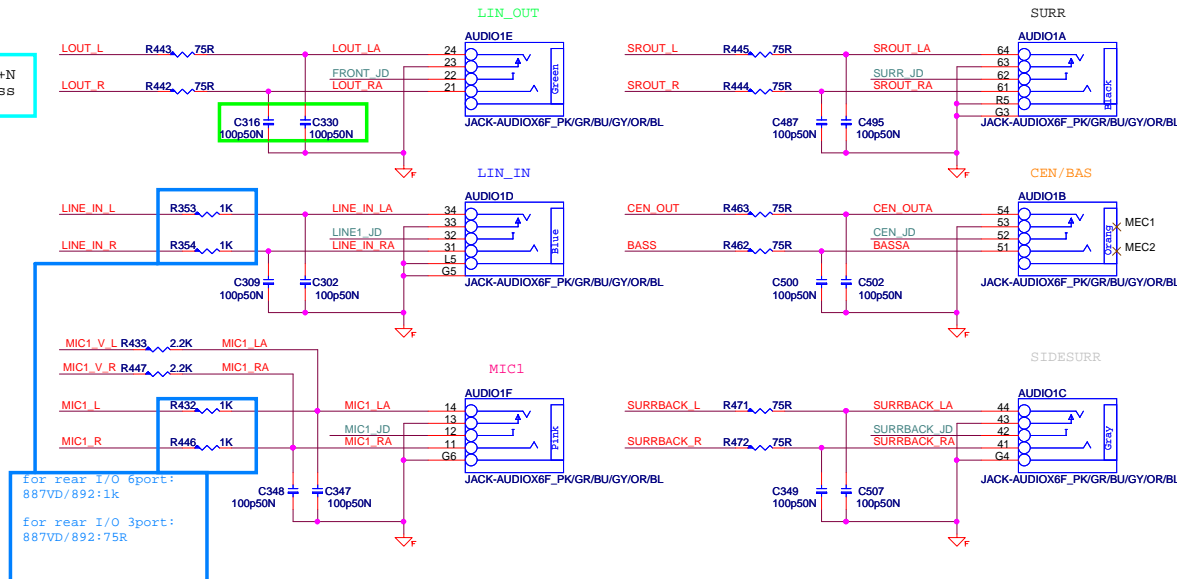
SPDIF OUT



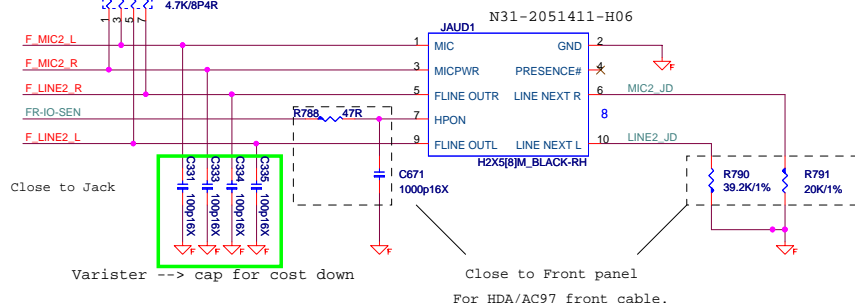
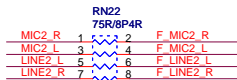
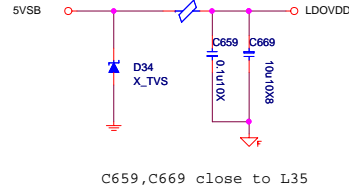
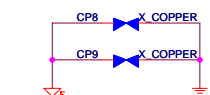
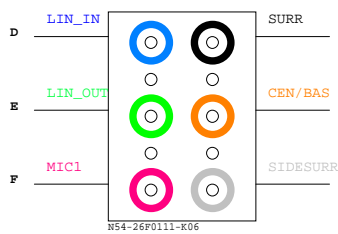
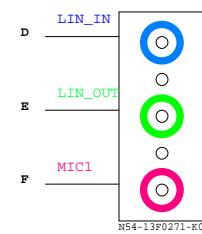
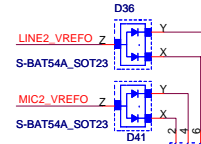
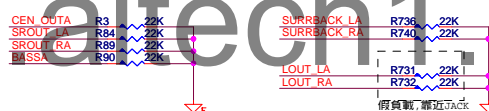
銅製程

銅製程

用SMD CAP 手動量測會FAIL在THD+N
用EL-CAP or SOLID cap, 才會pass

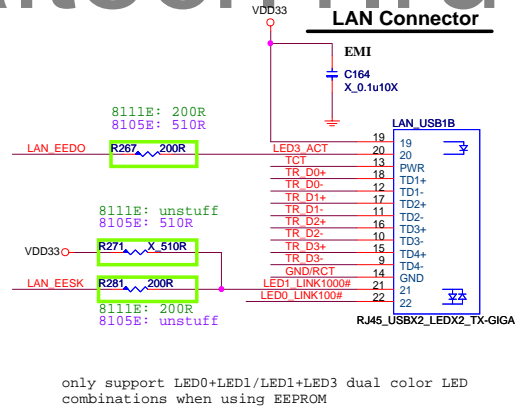
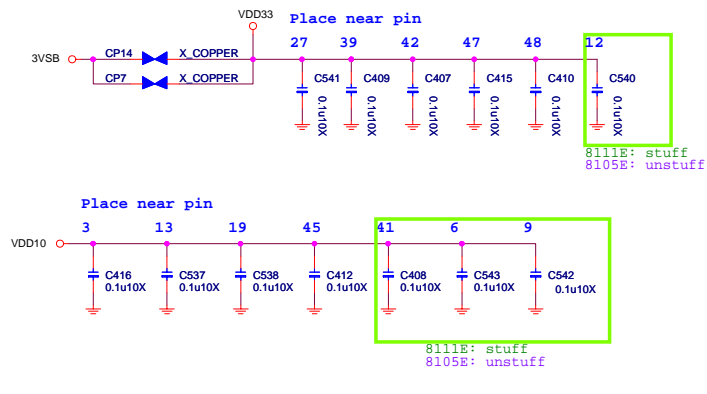
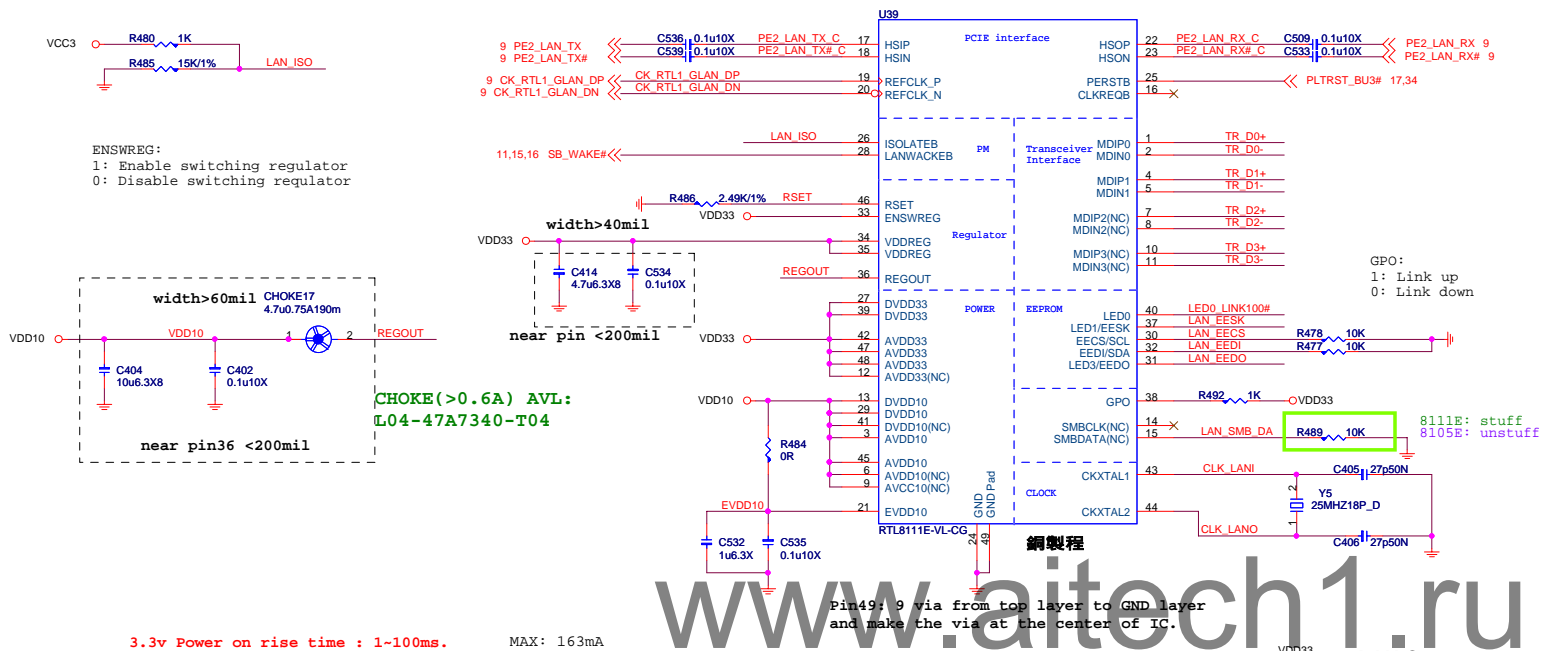


當串接電容有極性時，需上對地電阻



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MS-7756			
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RTL8105E 10/100M LAN

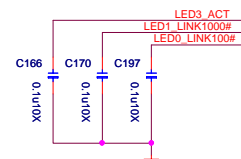


8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11



Giga-Lan	10/100-Lan																		
<p>N58-22F0731</p> <table><tr><td>Link</td><td>Yellow</td></tr><tr><td>Active</td><td>Blinking</td></tr><tr><td>1000</td><td>Orange</td></tr><tr><td>100</td><td>Green</td></tr><tr><td>10</td><td>None</td></tr></table>	Link	Yellow	Active	Blinking	1000	Orange	100	Green	10	None	<p>N58-22F0771</p> <table><tr><td>Link</td><td>Yellow</td></tr><tr><td>Active</td><td>Blinking</td></tr><tr><td>100</td><td>Green</td></tr><tr><td>10</td><td>None</td></tr></table>	Link	Yellow	Active	Blinking	100	Green	10	None
Link	Yellow																		
Active	Blinking																		
1000	Orange																		
100	Green																		
10	None																		
Link	Yellow																		
Active	Blinking																		
100	Green																		
10	None																		
<p>19</p> <p>20</p> <p>250R</p> <p>Yellow</p>	<p>19</p> <p>20</p> <p>Yellow</p>																		
<p>Orange</p> <p>21</p> <p>22</p> <p>250R</p> <p>Green</p>	<p>21</p> <p>22</p> <p>Green</p>																		

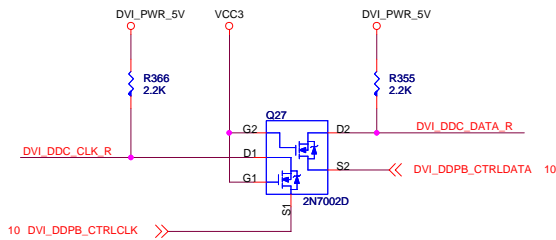
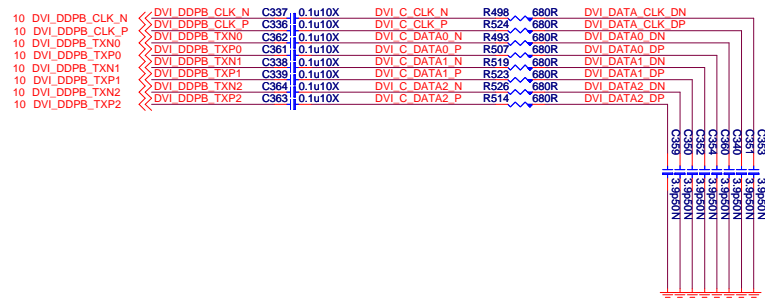


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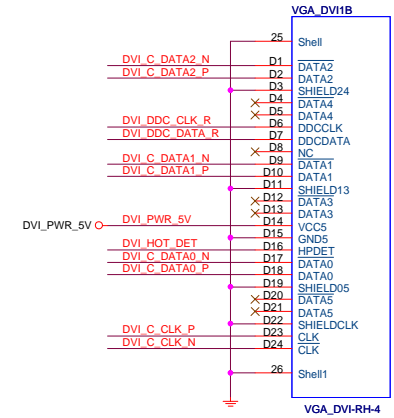
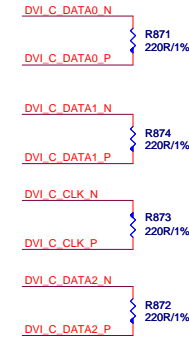
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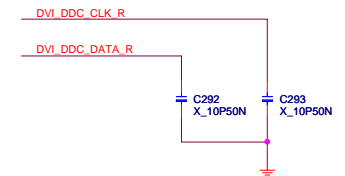
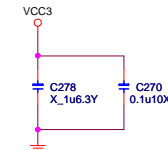
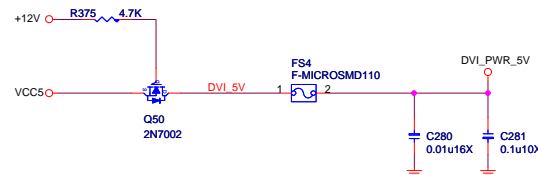
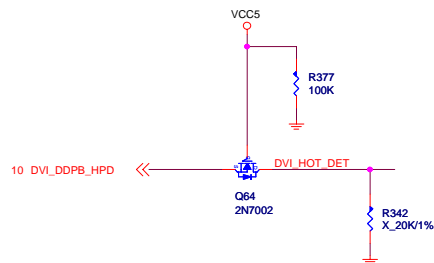
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



For EMI



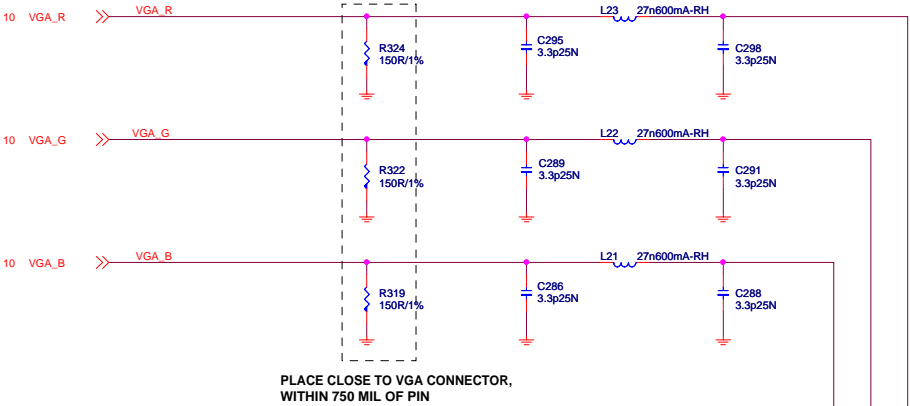
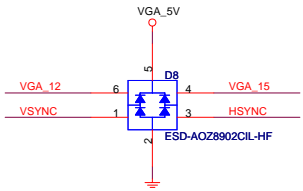
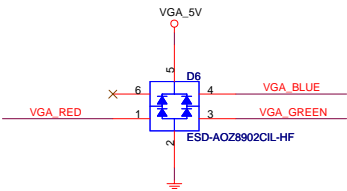
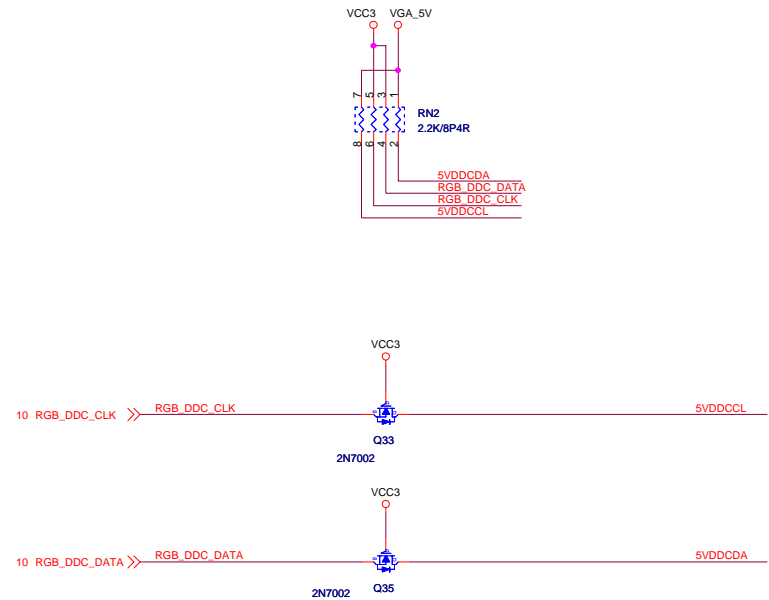
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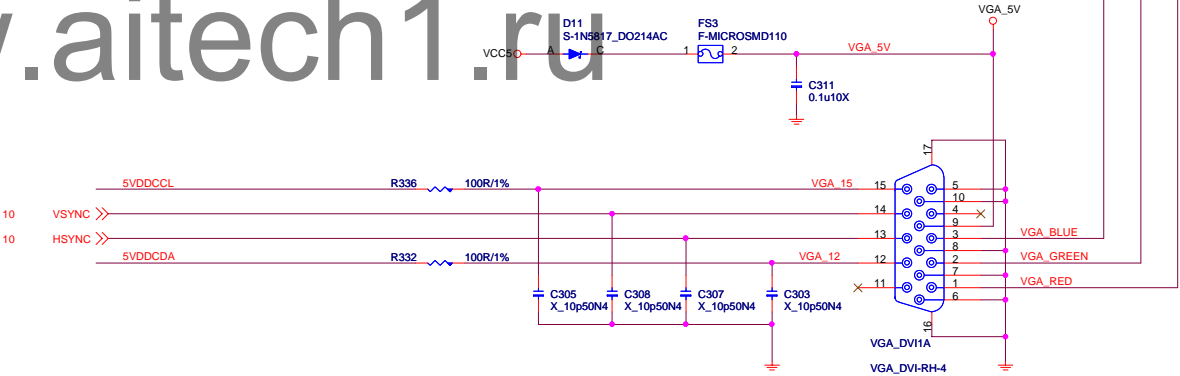
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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



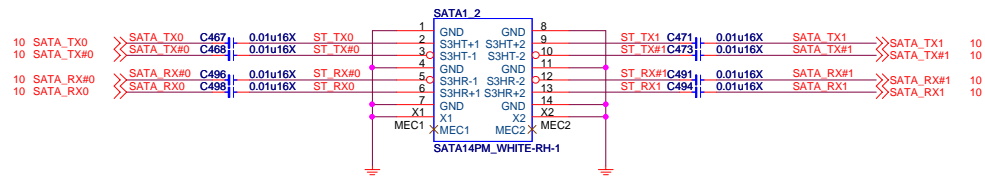
PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



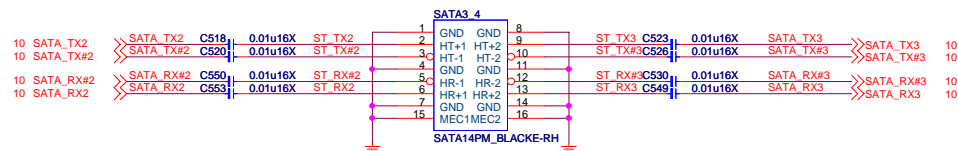
SATA1-2

3.0

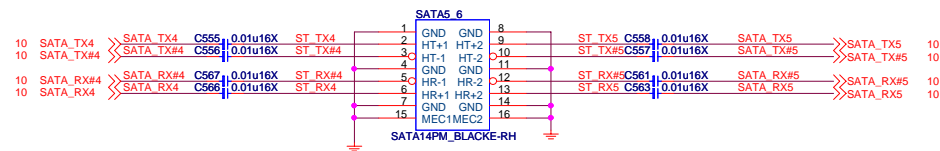
white



SATA3-4



SATA5-6



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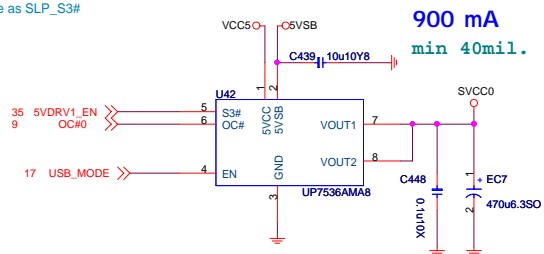


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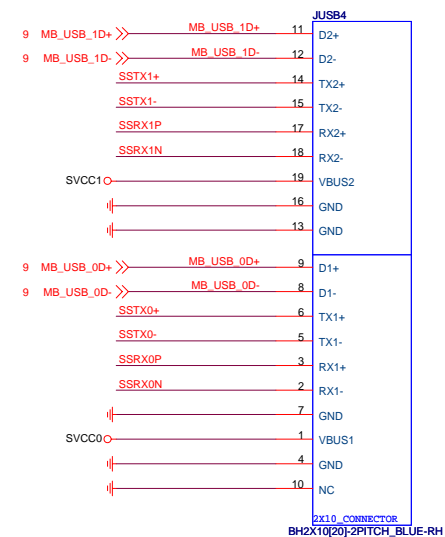
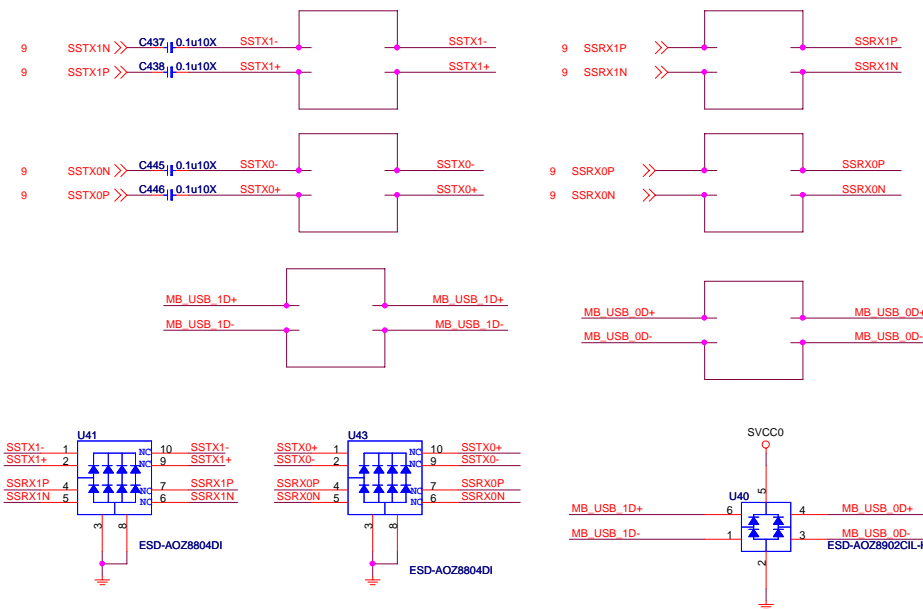
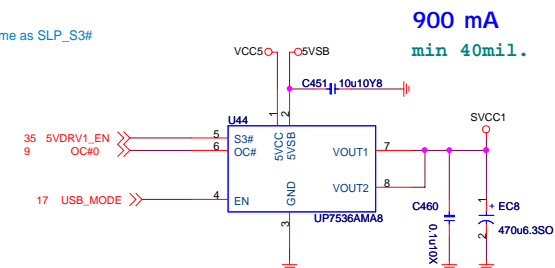
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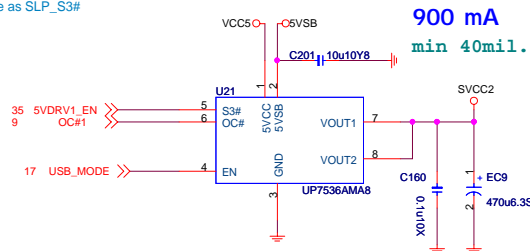
Same as SLP_S3#



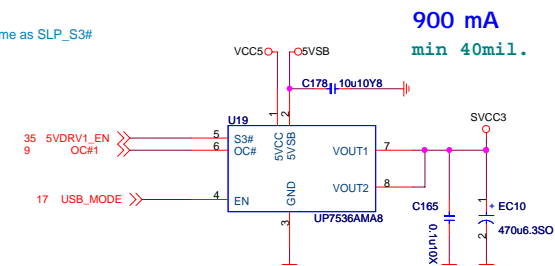
Same as SLP_S3#



Same as SLP_S3#

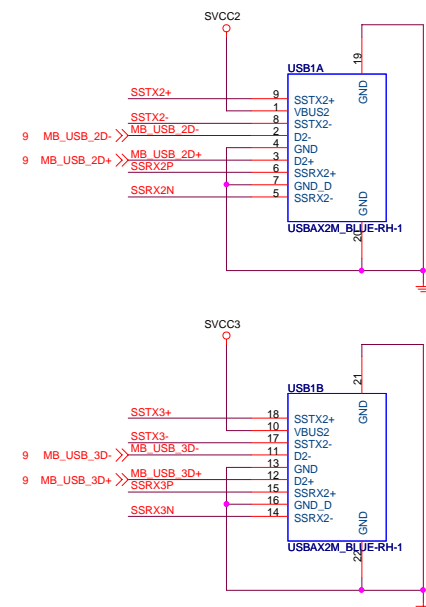
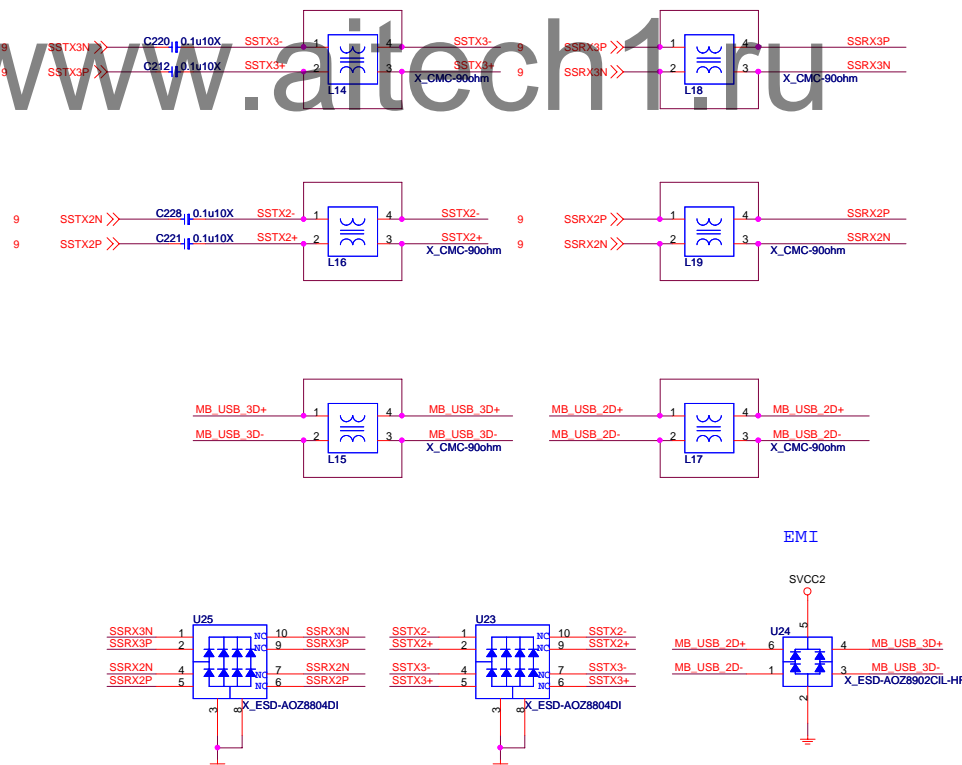


Same as SLP_S3#



```
USB_MODE
Hi by BIOS programing,
default h/w PD for avoid UP7536 Enable pin floating
```

MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



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Size Custom	Document Description USB3.0 Connector	Rev 1.0
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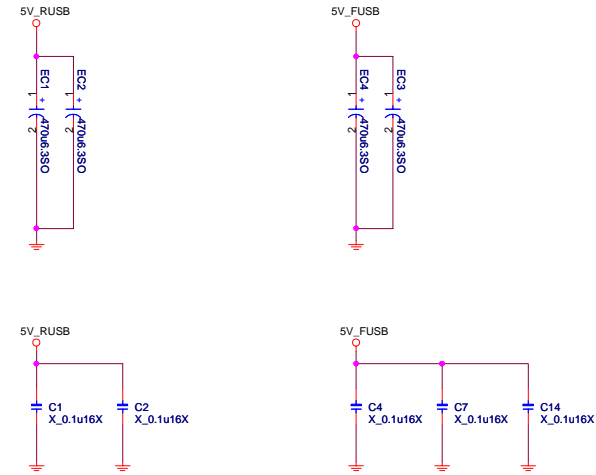
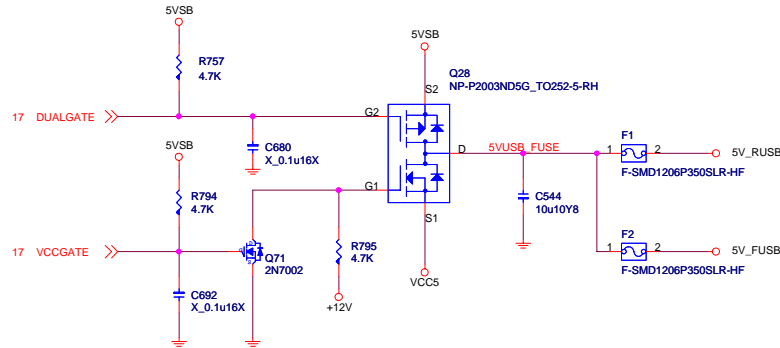
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0/1	1	0
S0P5_Gate#	1	0	1

When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

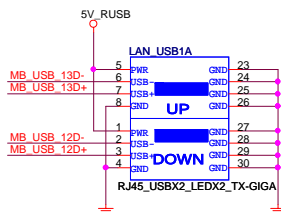
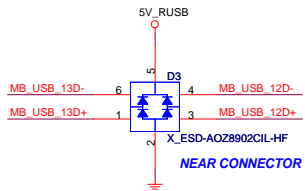
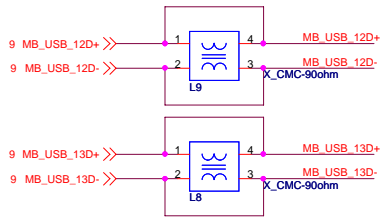
When PS2 in S5 support wake , S3P5_Gate# in S5 must setting to Low

*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

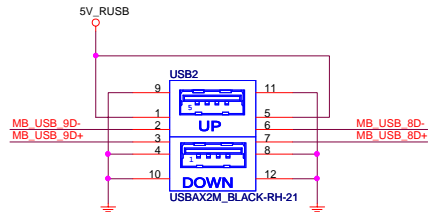
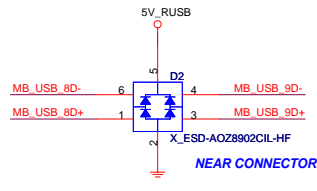
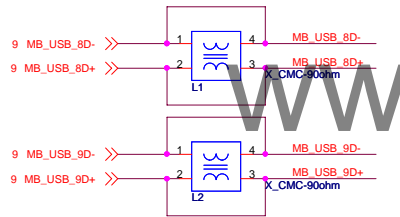
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



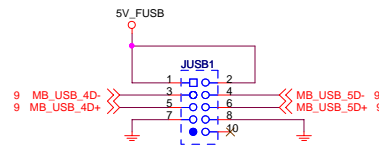
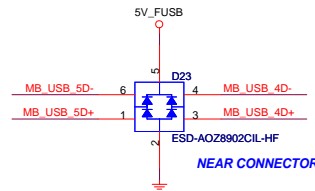
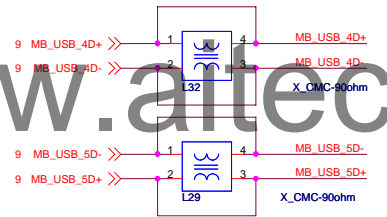
REAR USB PORT 8,9 (With PS2)



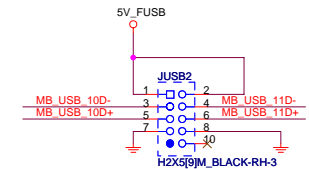
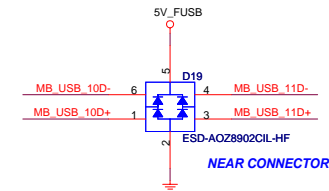
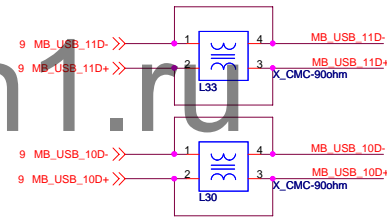
REAR USB PORT 8,9 (With PS2)



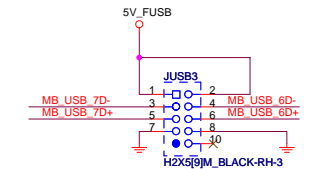
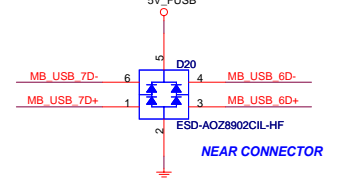
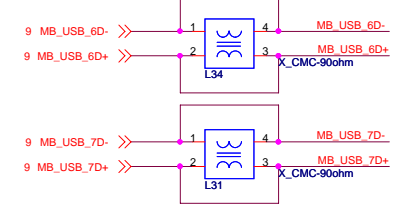
FRONT USB PORT 0,1



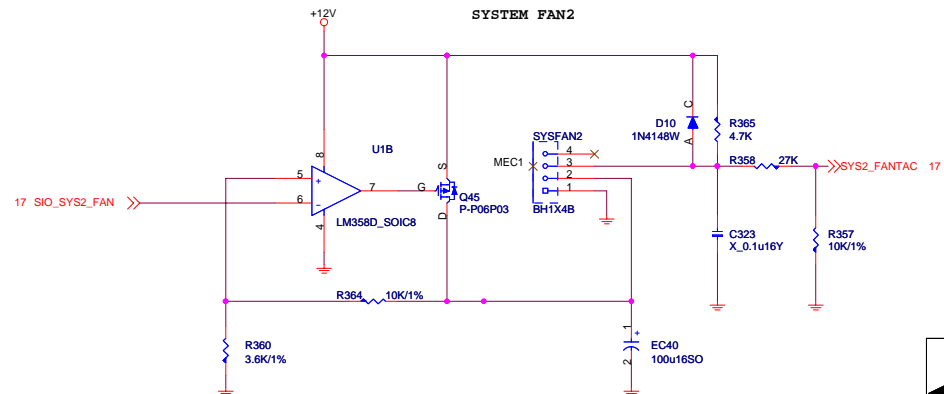
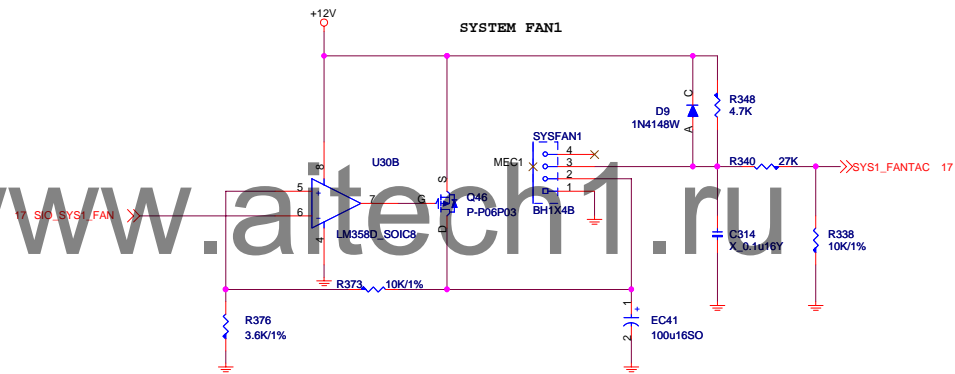
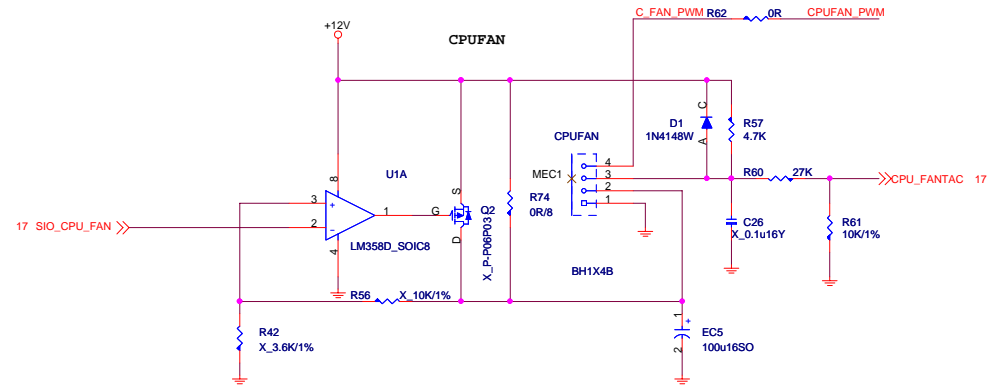
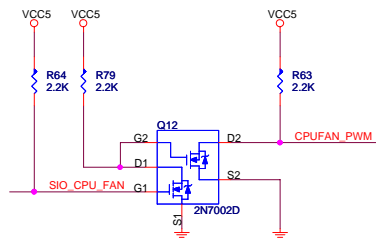
FRONT USB PORT 8,9



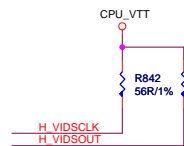
FRONT USB PORT 10,11



FAN-COUNTROL CIRCUIT



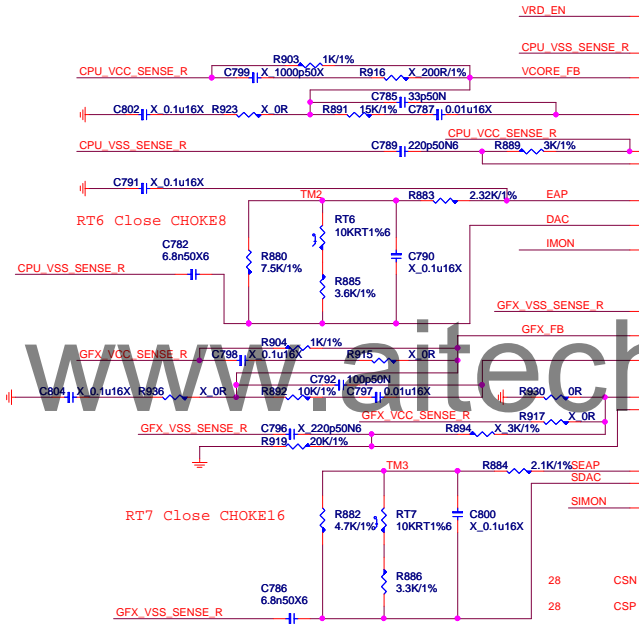
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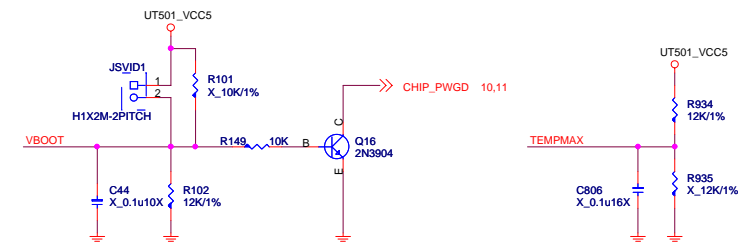
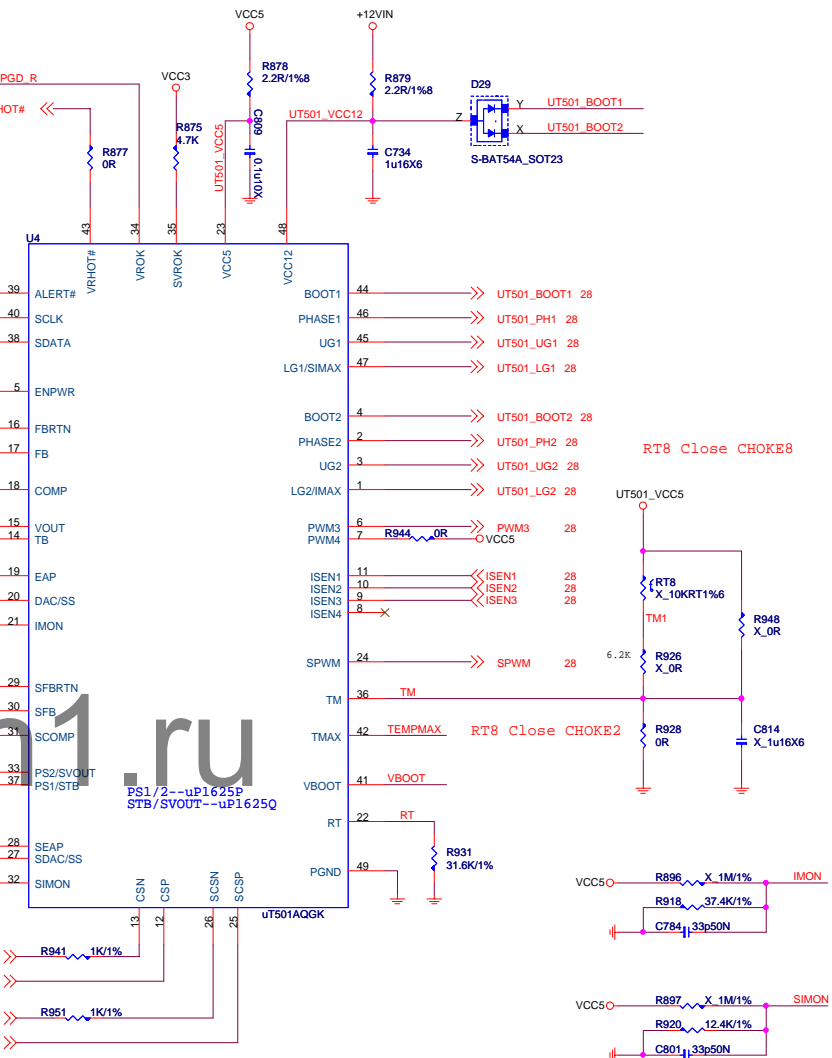
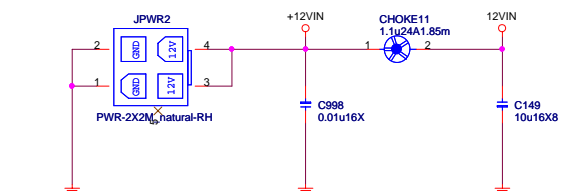
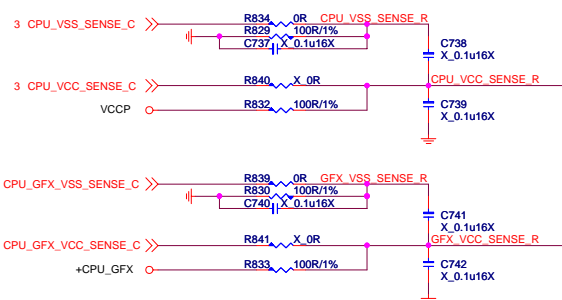
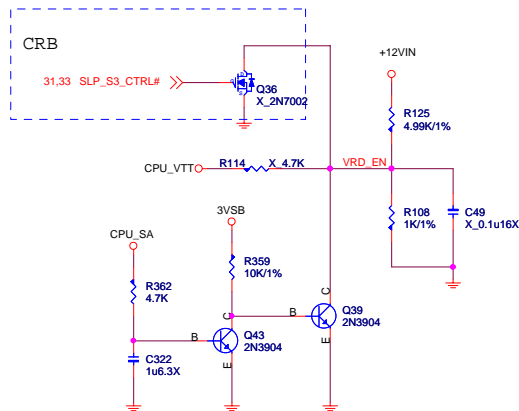
3 VID_ALERT#

3 H_VIDCLK

3 H_VIDSOUT

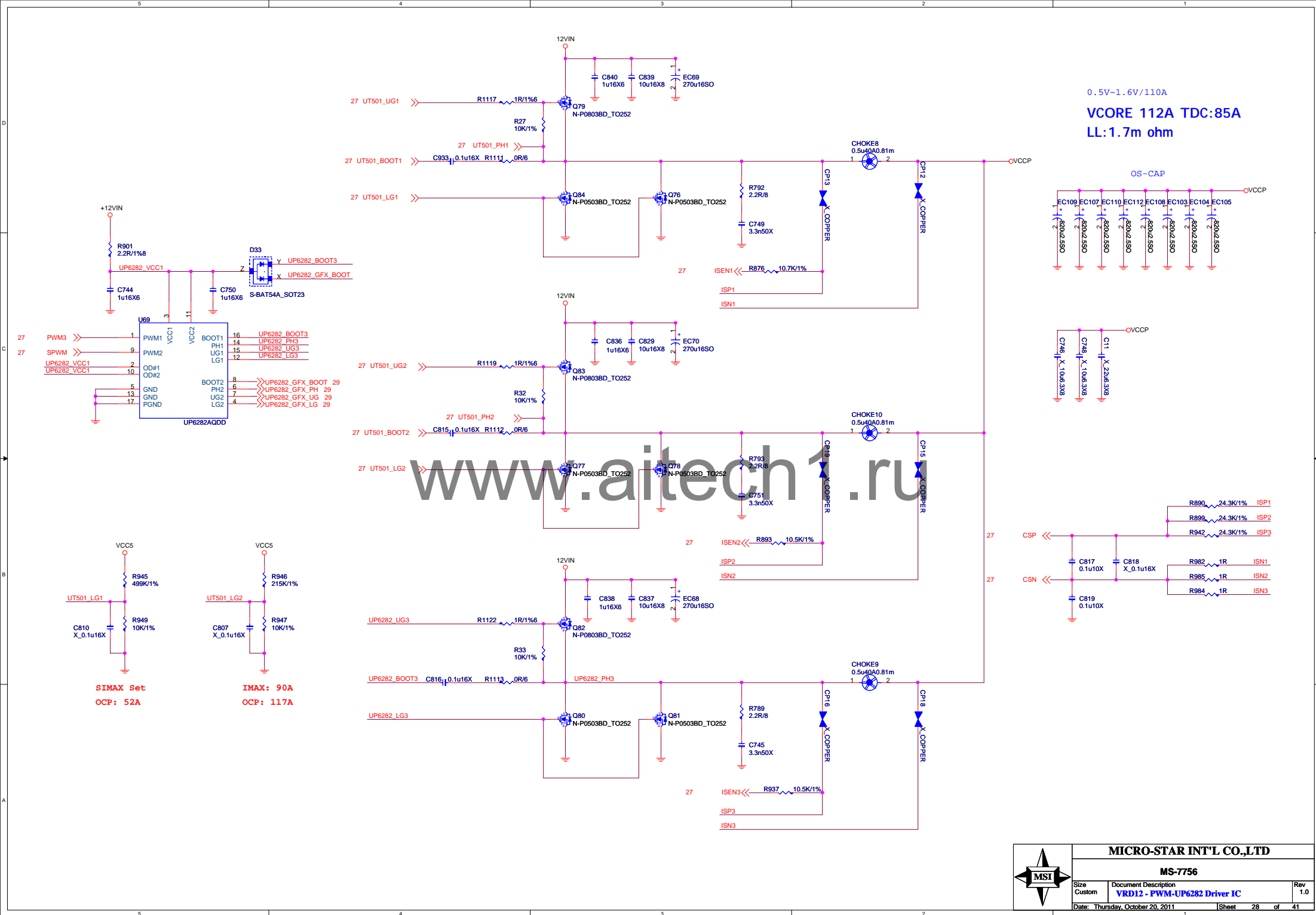


0x20: RH=10K, RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



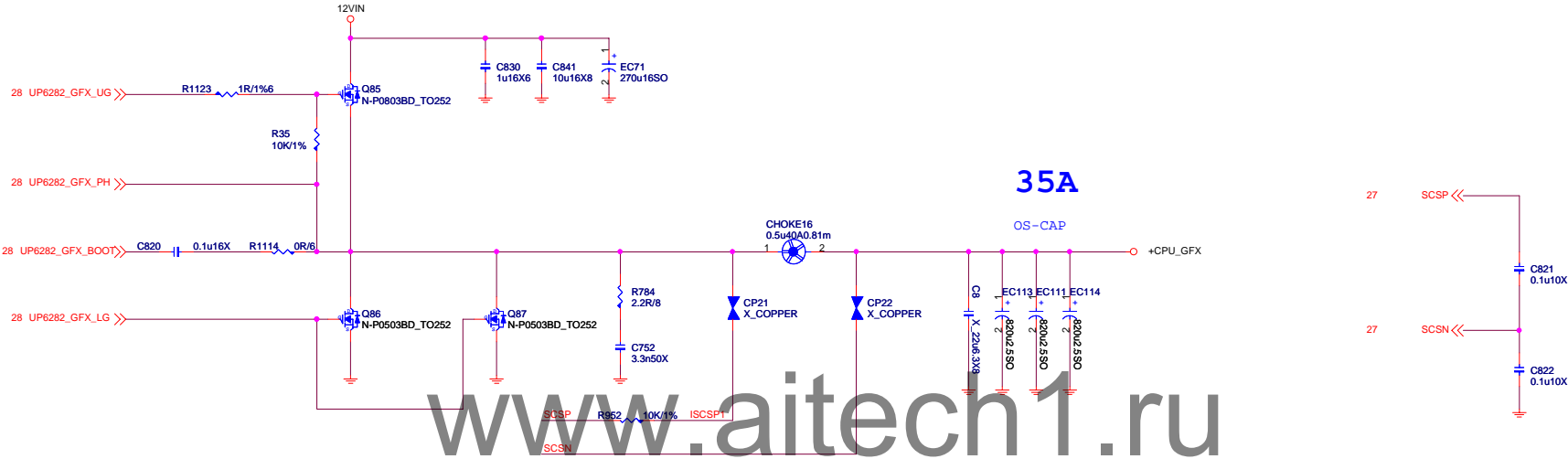
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CPU_GFX:0.25-1.52

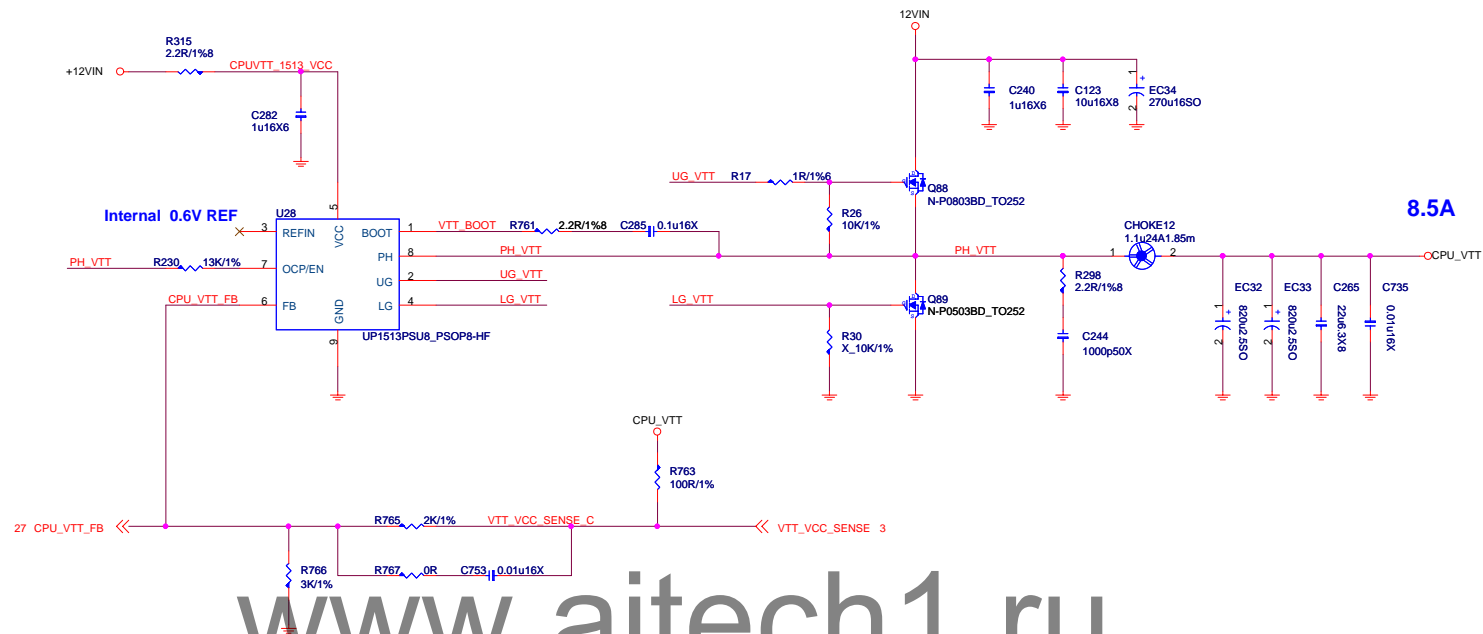
35A FOR CPU



8.5A FOR CPU

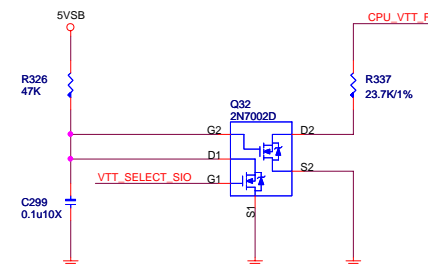
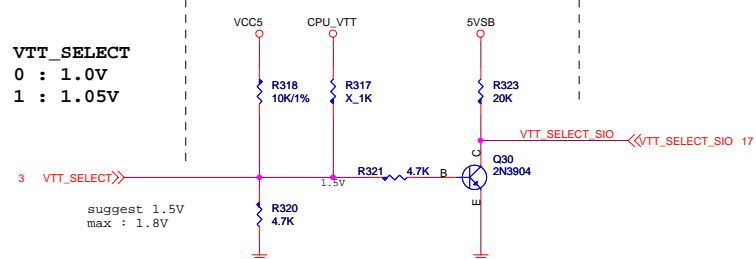
$$I_{ripple} = 1.92(v_{tt}) + 1.88(s_a)$$

$$5 \times 1 = 5A > 3.8A$$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



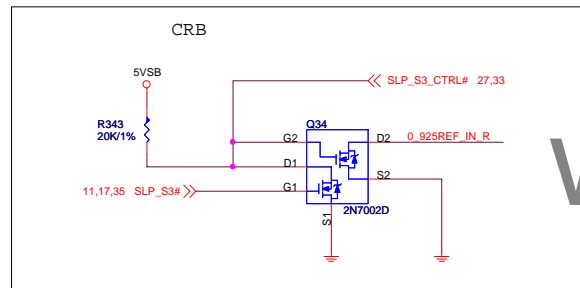
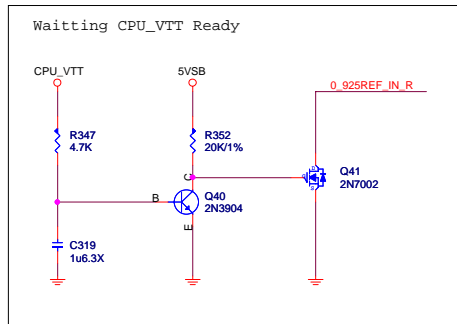
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Size Custom	Document Description VTT POWER- uP1513- 1Phase MOS	Rev 1.0
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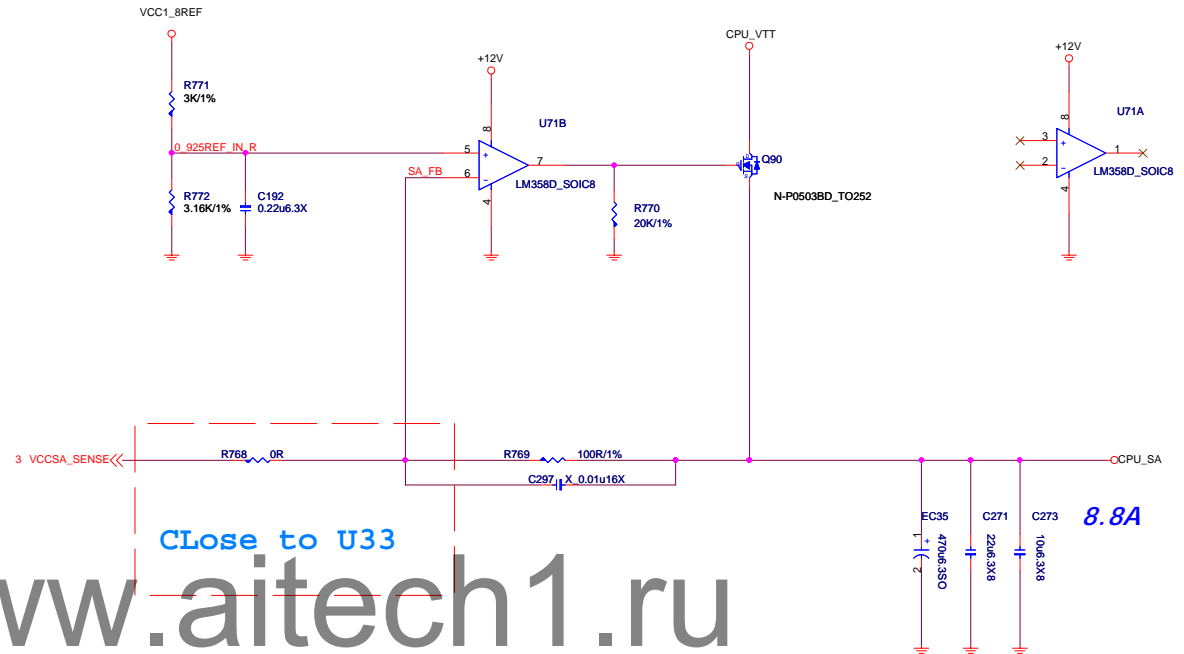
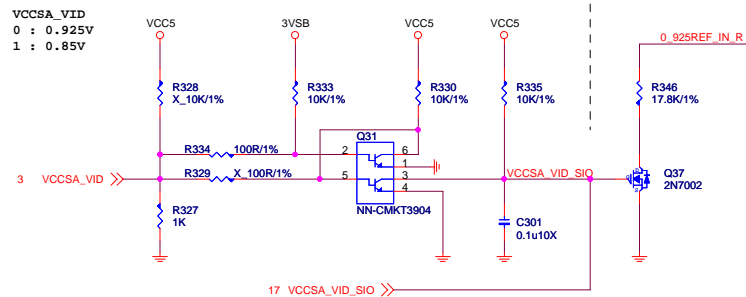
CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



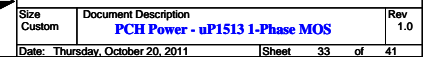
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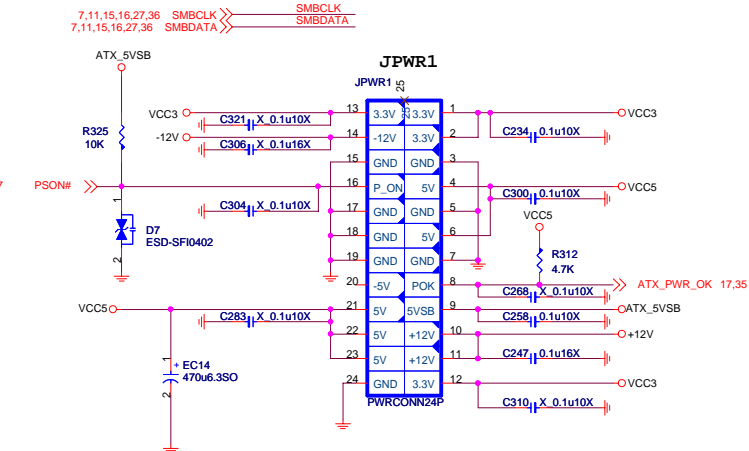
Size	Document Description	Rev
Custom	CPU_SA OP+MOS 1-Phase	1.0
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Size Custom	Document Description DDR Power -UP1513 1-Phase MOS	Rev 1.0
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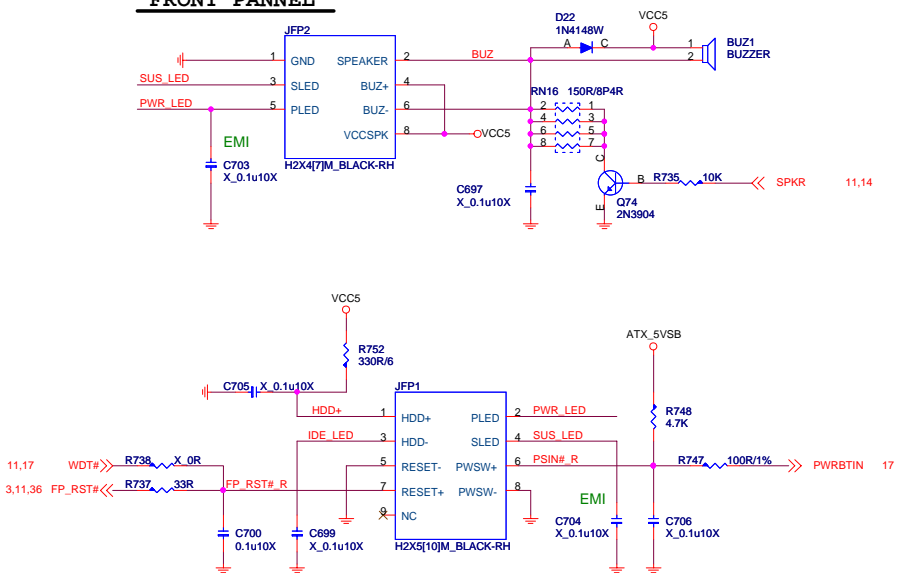
1.8A FOR ME CORE



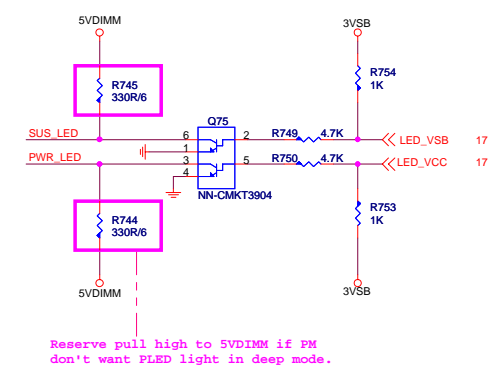
ATX POWER CONNECTOR



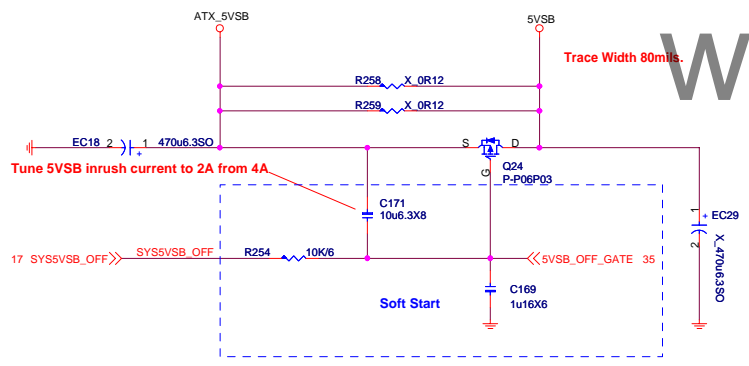
FRONT PANEL



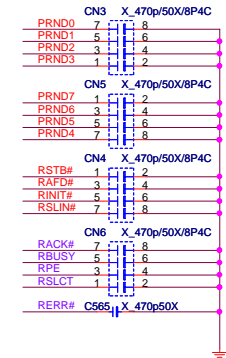
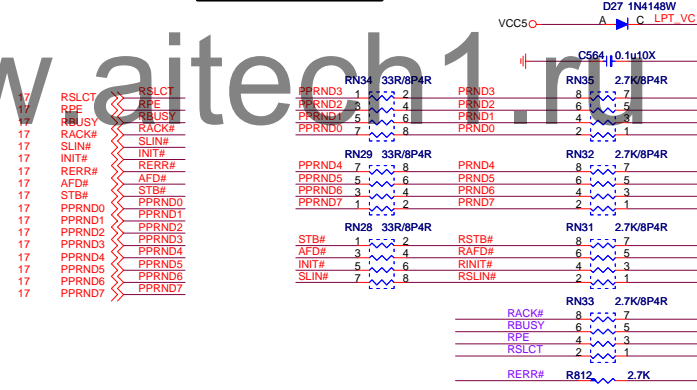
LED (for Fintek 71869)



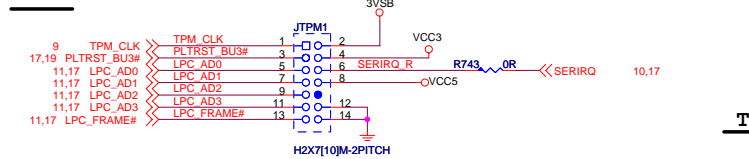
5VSB Power Switch



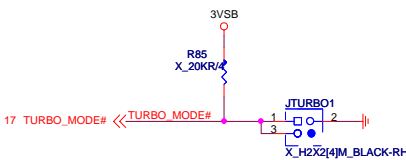
PARALLAL PORT



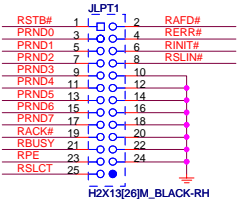
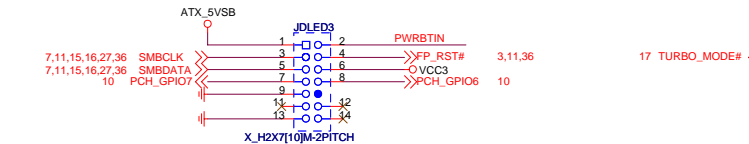
TPM



Turbo Button

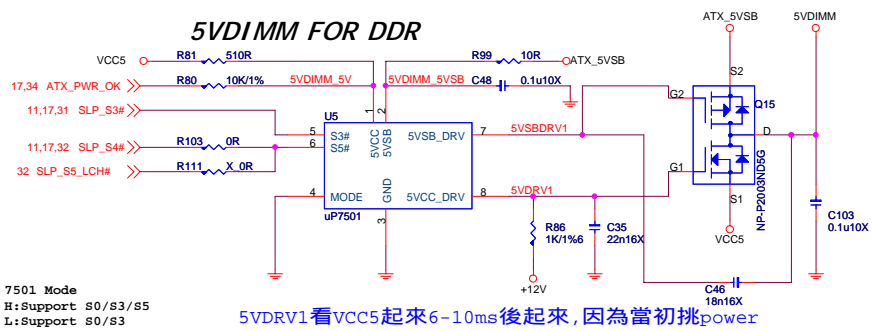


JDLED3

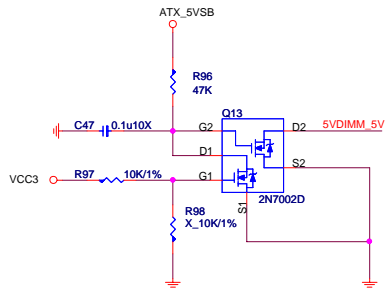
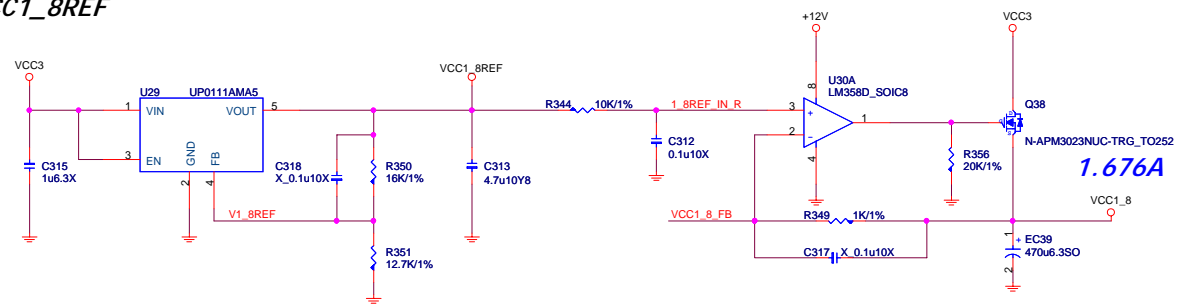


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Custom	ATX F_Panel/EMI/TPM	1.0	
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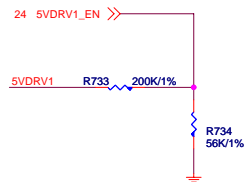
5VDIMM FOR DDR



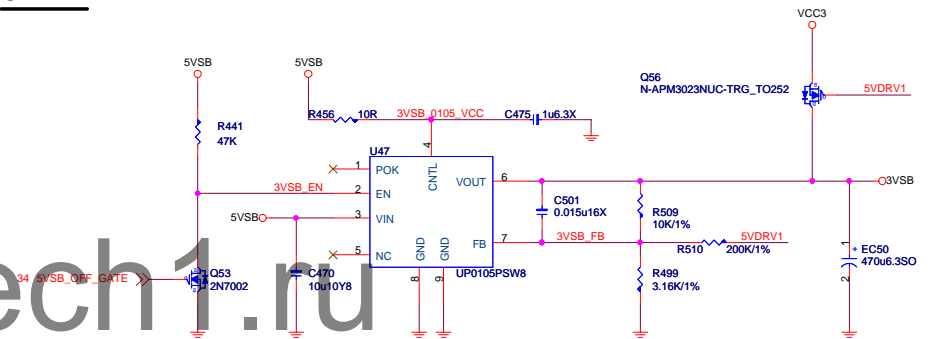
VCC1_8REF



USB MODE

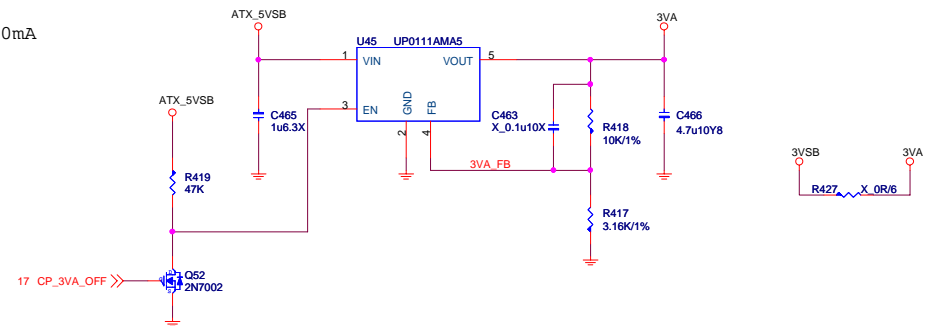


3VSB



3VA

20mA

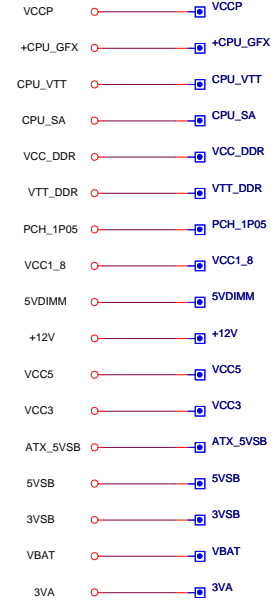


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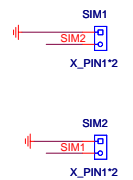
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Custom	ACPI controller UPI	1.0
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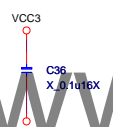
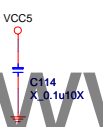
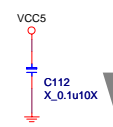
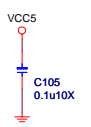
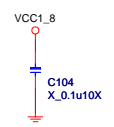
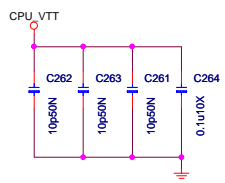
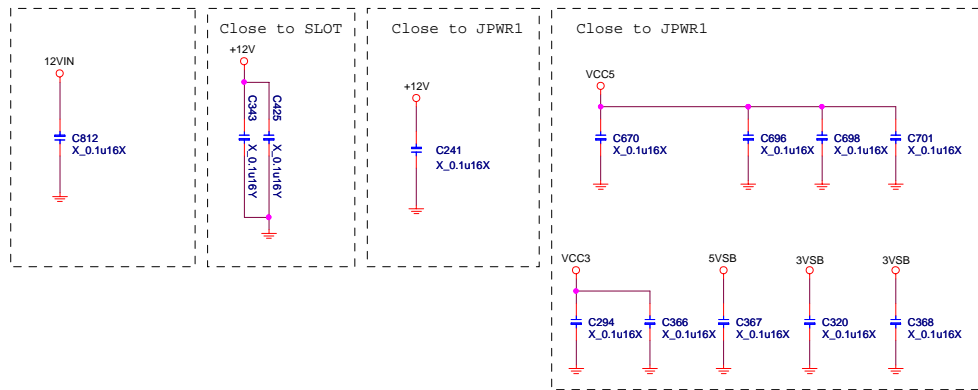
Voltage test point



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